General Description

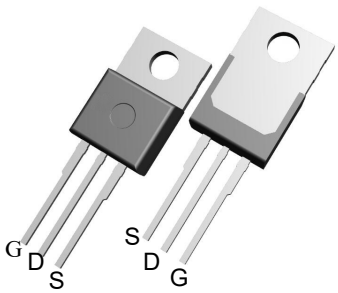
MY80N06P used N-channel Enhanced VDMOSFET, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

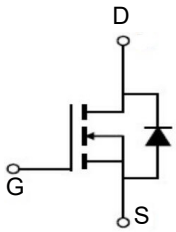
Features

V_{DSS}	60	V
I_D	80	A
$R_{DS(ON)}$(atV_{GS} =10V)	6.5	mΩ
$R_{DS(ON)}$(atV_{GS} =4.5V)	10	mΩ

Application

- Battery protection
- Load switch
- Uninterruptible power supply





Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY80N06P	TO-220	80N06P	1000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [G]	T_C=25°C	I_D	80	A
	T_C=100°C		60	
Pulsed Drain Current [C]		I_{DM}	184	
Continuous Drain Current	T_A=25°C	I_{DSM}	14	A
	T_A=70°C		11	
Avalanche Current [C]		I_{AS}	60	A
Avalanche energy	L=0.1mH [C]	E_{AS}	180	mJ
V_{DS} Spike	10μs	V_{SPIKE}	72	V
Power Dissipation [B]	T_C=25°C	P_D	150	W
	T_C=100°C		75	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2.5	W
	T_A=70°C		1.6	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	16	20	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		41	50	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	0.8	1.0	°C/W

Electrical Characteristics at T_j=25 ℃ unless otherwise specified

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V		60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V				1	μA
			T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V				±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA		1.7	2.5	3.2	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=12A			6.5	8.5	mΩ
			T_J=125°C		10	12	
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A			75		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V			0.7	1	V
I_S	Maximum Body-Diode Continuous Current G					46	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=30V, f=1MHz			4050		pF
C_{oss}	Output Capacitance				345		pF
C_{rss}	Reverse Transfer Capacitance				16.8		pF
R_g	Gate resistance	f=1MHz		0.3	0.65	1.0	Ω
SWITCHING PARAMETERS							
$Q_{g(10V)}$	Total Gate Charge	V_{GS}=10V, V_{DS}=30V, I_D=20A			53	75	nC
$Q_{g(4.5V)}$	Total Gate Charge				22	31	nC
Q_{gs}	Gate Source Charge				17		nC
Q_{gd}	Gate Drain Charge				5		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=30V, R_L=1.5Ω, R_{GEN}=3Ω			18		ns
t_r	Turn-On Rise Time				20		ns
$t_{D(off)}$	Turn-Off DelayTime				33		ns
t_f	Turn-Off Fall Time				4		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/μs			26		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/μs			125		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25。C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150。C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175。C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175。C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature $T_{J(MAX)}$=175。C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175。C. The SOA curve provides a single pulse rating.

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25。C.

Typical Characteristics

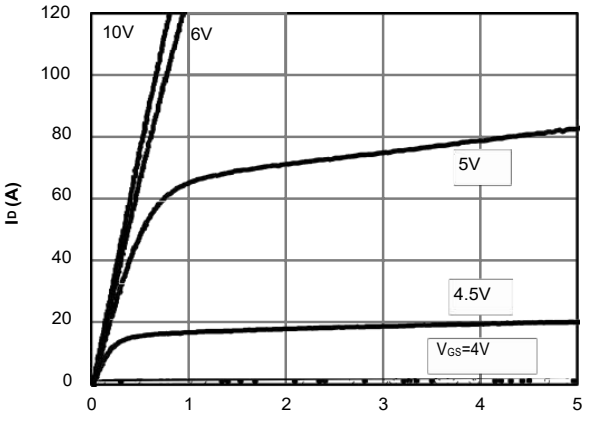


Figure 1: On-Region Characteristics (Note E)

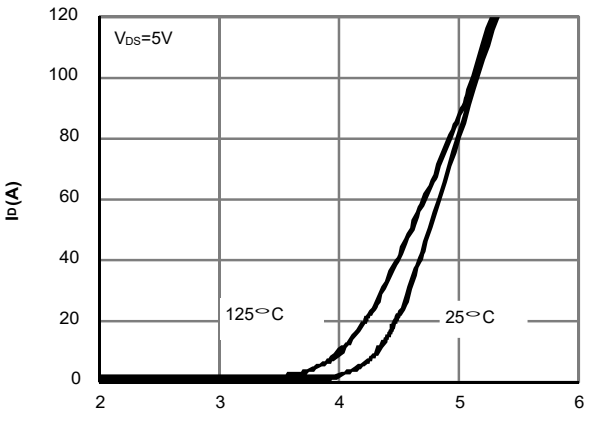


Figure 2: Transfer Characteristics (Note E)

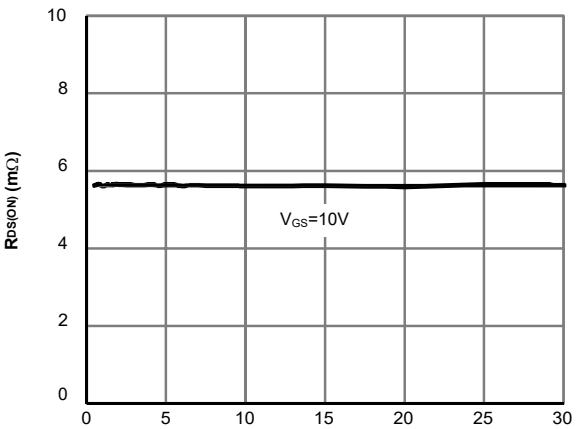


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

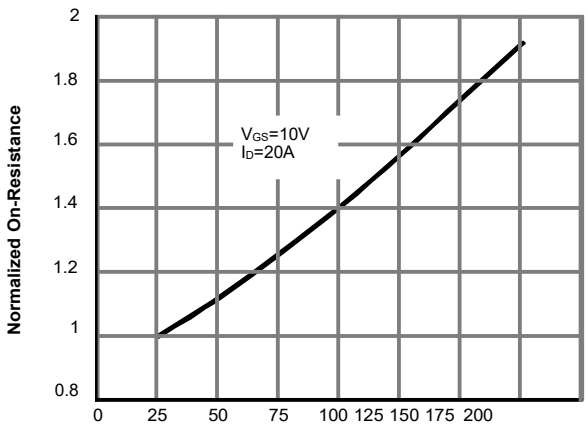


Figure 4: On-Resistance vs. Junction Temperature (Note E)

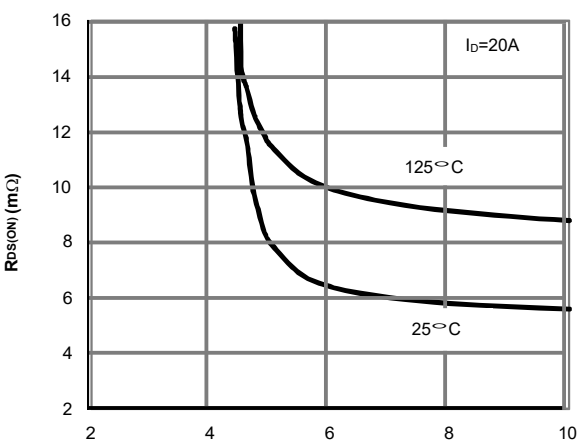


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

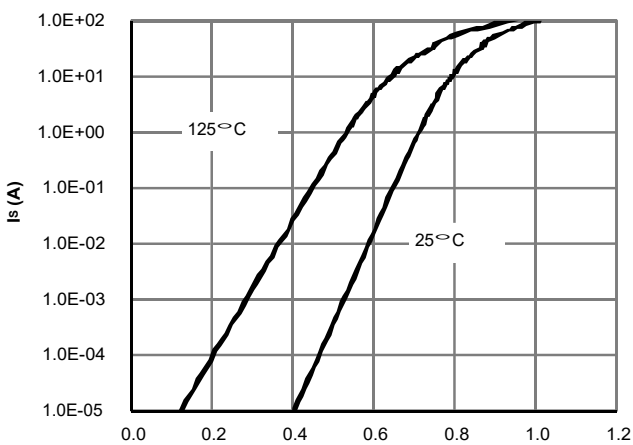


Figure 6: Body-Diode Characteristics (Note E)

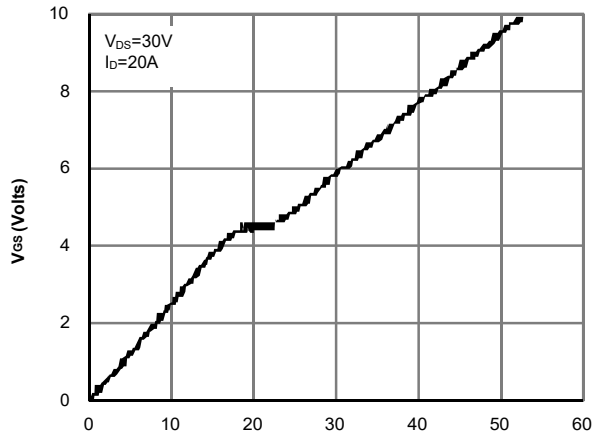


Figure 7: Gate-Charge Characteristics

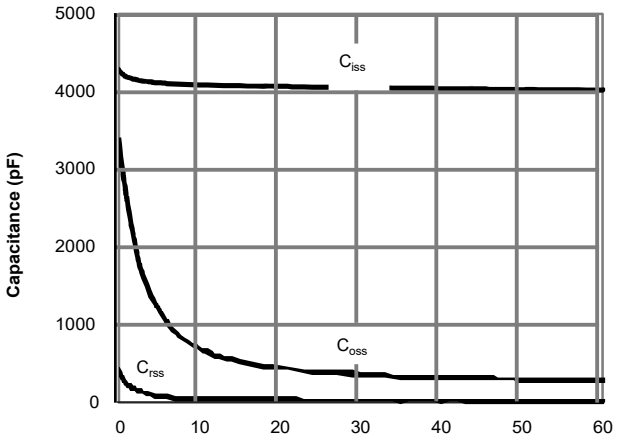


Figure 8: Capacitance Characteristics

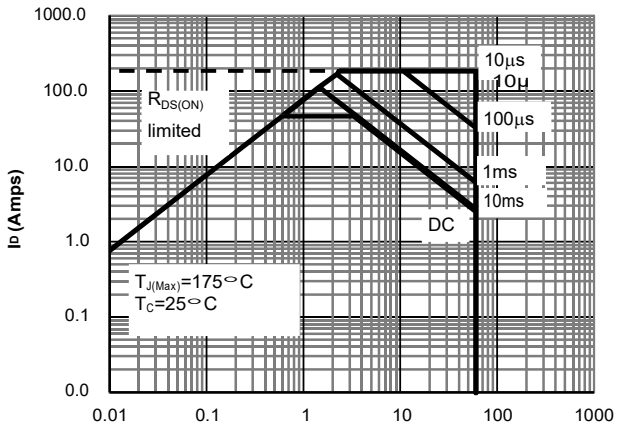


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

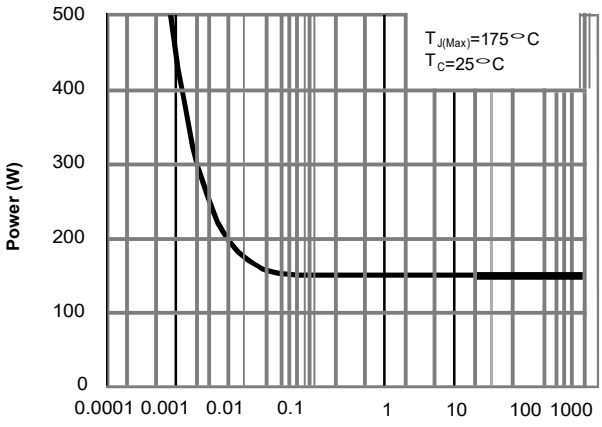


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

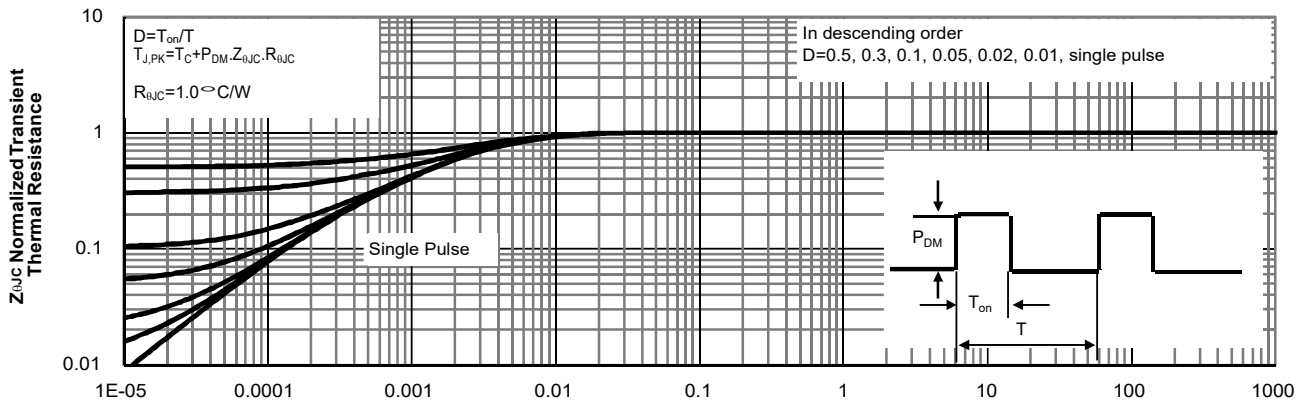


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

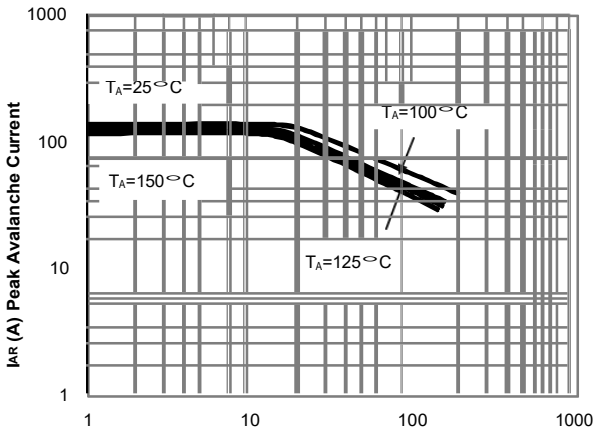


Figure 12: Single Pulse Avalanche capability (Note C)

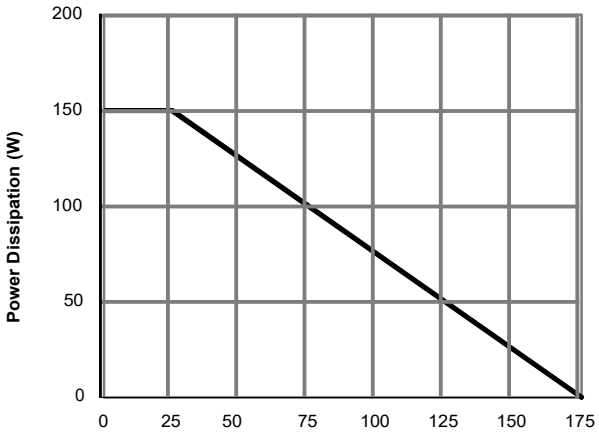


Figure 13: Power De-rating (Note F)

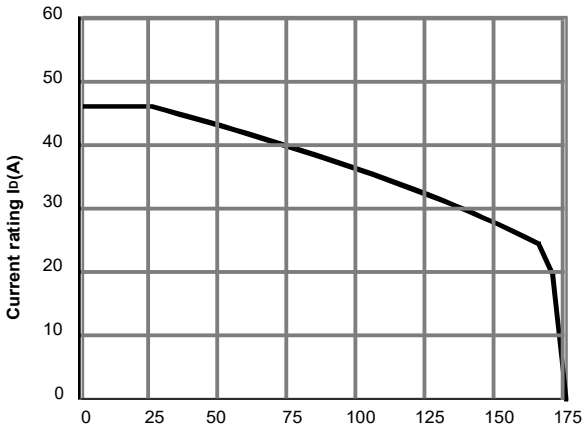


Figure 14: Current De-rating (Note F)

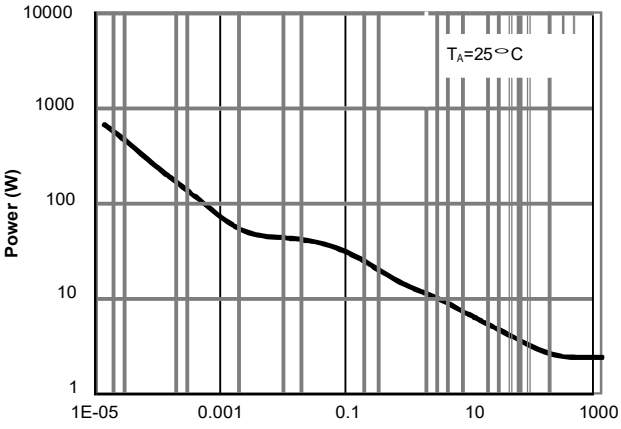


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

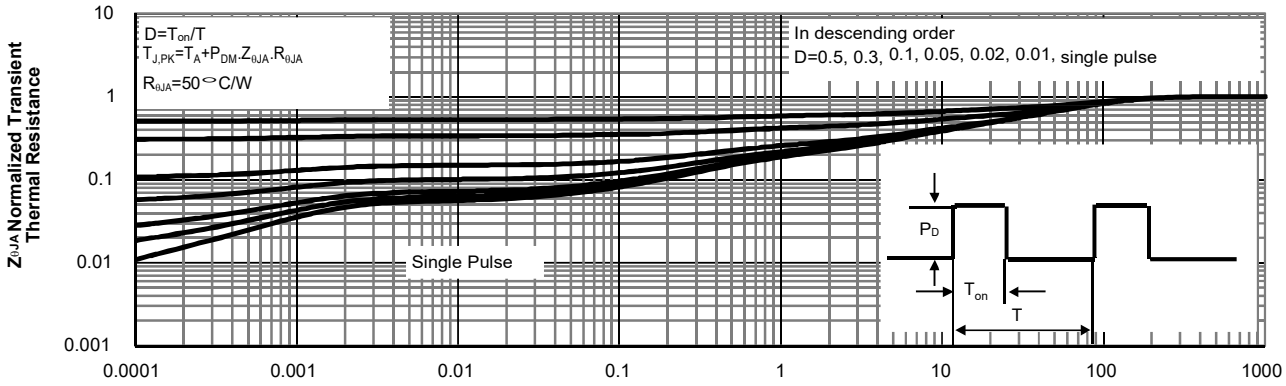
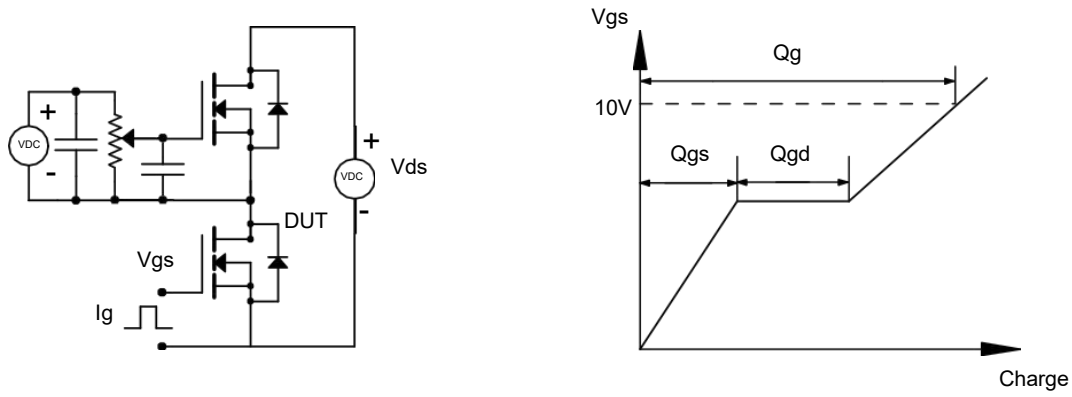
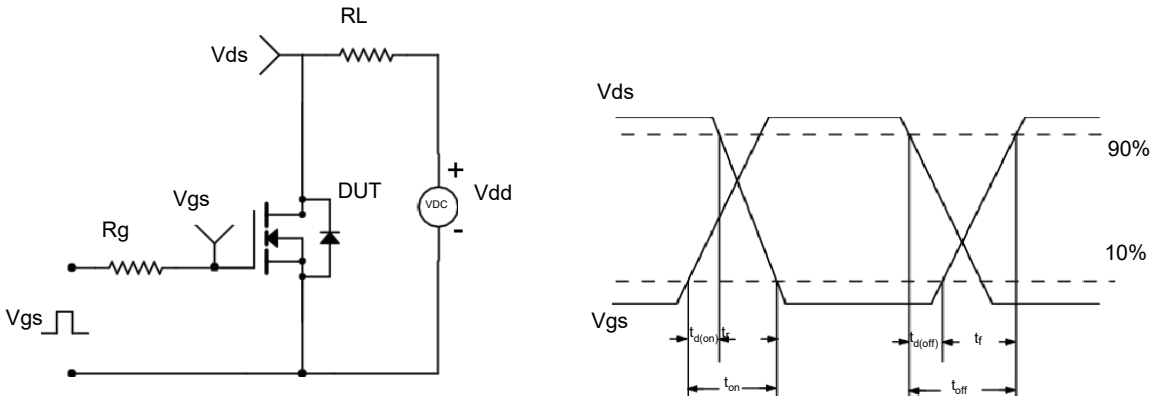


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H

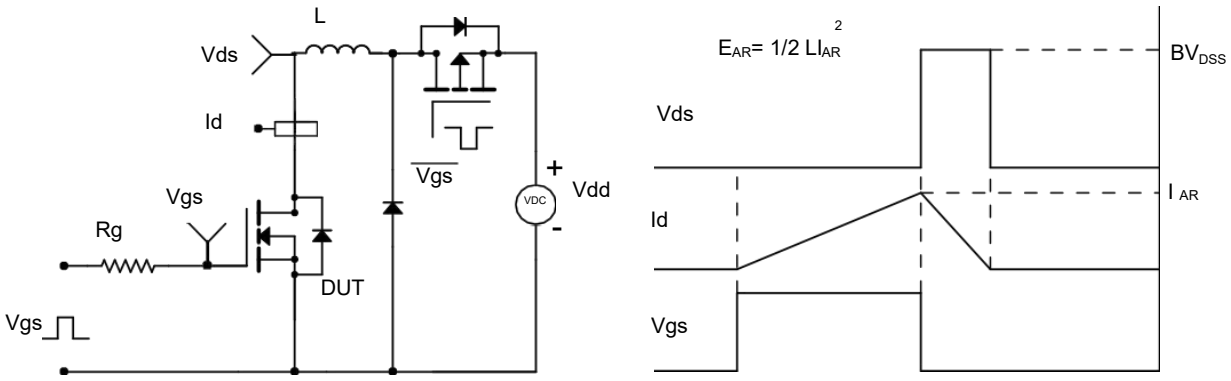
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms