MY7N50D

500V N-Channel Enhancement Mode MOSFET

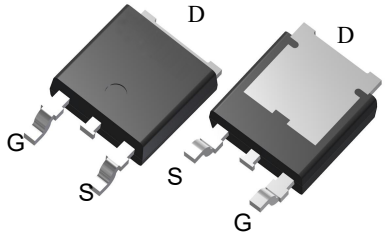
MAOYUANWEI semiconductor

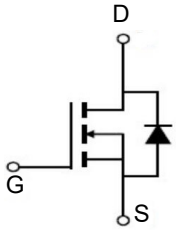
General Description

The MY7N50D uses silicon N-channel Enhanced VDMOSFETs, is obtained by the Synchronus Rectification Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-252, which accords with the RoHS standard.

Features

V_{DSS}	500	V
I_D	7	A
$P_D(T_C=25℃)$	79	W
$R_{DS(ON)}$(atV_{GS}=10V)	90	mΩ





Application

- Fast Switching
- Low ON Resistance
- Low Gate Charge

Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY7N50D	TO-252	MY7N50D	2500

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	500	V
I_D	Continuous Drain Current T_C = 25 ℃	7	A
	Continuous Drain Current T_C = 100 ℃	4.6	A
I_{DM} [a1]	Pulsed Drain Current T_C = 25 ℃	28	A
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS} [a2]	Single Pulse Avalanche Energy	282	mJ
dv/dt [a3]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation T_C = 25 ℃	79	W
	Derating Factor above 25℃	0.6	W/℃
$V_{ESD(G-S)}$	Gate source ESD (HBM-C= 100pF, R=1.5kΩ)	3000	V
T_J，T_{stg}	Operating Junction and Storage Temperature Range	150，–55 to 150	℃

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	500	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	ID=250uA,Reference25℃	--	0.55	--	V/℃
I_{DSS}	Drain to Source Leakage Current	V_{DS} =500V, V_{GS}= 0V, Tj = 25℃	--	--	1	μA
		V_{DS} =400V, V_{GS}= 0V, Tj = 125℃	--	--	100	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS} =+20V	--	--	10	μA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS} =-20V	--	--	-10	μA

ON Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=3.5A	--	90	110	mΩ
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	3.5	--	4.5	V
Pulse width tp≤300μs,δ≤2%						

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	V_{DS}=20V, I_D =3.5A	--	6.0	--	S
R_g	Gate resistance	f = 1.0MHz	--	4.7	--	Ω
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} = 100V f = 1.0MHz	--	860	--	PF
C_{oss}	Output Capacitance		--	39	--	
C_{rss}	Reverse Transfer Capacitance		--	3.5	--	

Resistive Switching Characteristics

Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D =7A V_{DD} = 250V V_{GS} = 10V R_G =10Ω	--	17.6	--	ns
tr	Rise Time		--	16.8	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	27.6	--	
t_f	Fall Time		--	14.2	--	
Q_g	Total Gate Charge	I_D =7A V_{DD} =400V V_{GS} = 10V	--	19.7	--	nC
Q_{gs}	Gate to Source Charge		--	4.8	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	9.3	--	
Vp	Platform Voltage			5.9		V

Typical Characteristics

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)	T_C = 25 ℃	--	--	7	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	28	A
V_{SD}	Diode Forward Voltage	I_S=7A,V_{GS}=0V	--	--	1.5	V
T_{rr}	Reverse Recovery Time	I_S=7.0A,T_j = 25℃ dI$_F$/dt=100A/us, V_{GS}=0V	--	60	--	ns
Q_{rr}	Reverse Recovery Charge		--	95	--	nC
I_{rrm}	Reverse Recovery Current		--	3.2	--	A
Pulse width tp≤300μs,δ≤2%						

Symbol	Parameter	Max.	Units
$R_{\theta JC}$	Junction-to-Case	1.58	℃/W
$R_{\theta JA}$	Junction-to-Ambient	100	℃/W

Gate-source Zener diode						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{GSO}	Gate-source breakdown voltage	I_{GS}= ±1mA(Open Drain)	30			V
The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.						

[a1]: Repetitive rating; pulse width limited by maximum junction temperature [a2]:

L=10mH, I_D=7.5A, Start T_J=25℃

[a3]: I_{SD} =7A,di/dt ≤100A/us,V_{DD}≤$BV_{DS,}$ Start T_J=25℃

[a4]: Recommend soldering temperature defined by IPC/JEDEC J-STD 020

Characteristics Curve:

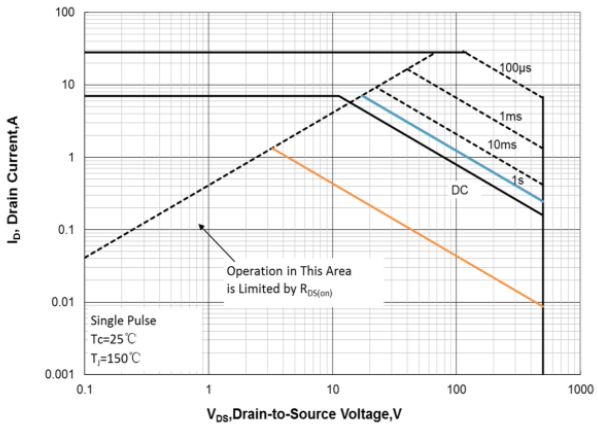


Figure 1 Maximum Forward Bias Safe Operating Area

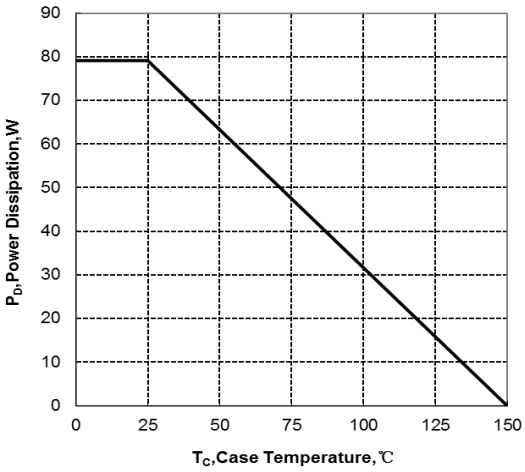


Figure 2 Maximum Power dissipation vs Case Temperature

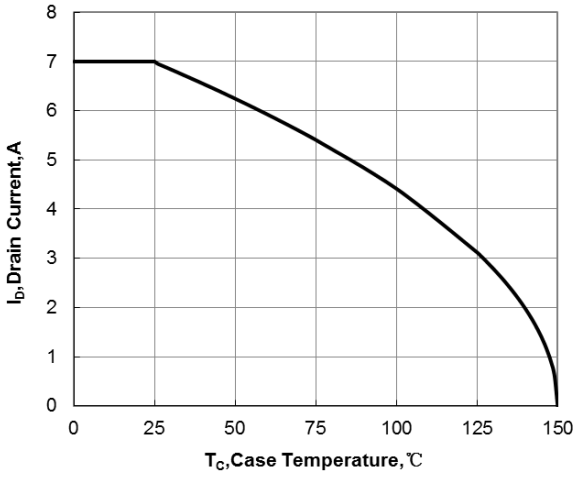


Figure 3 Maximum Continuous Drain Current vs Case Temperature

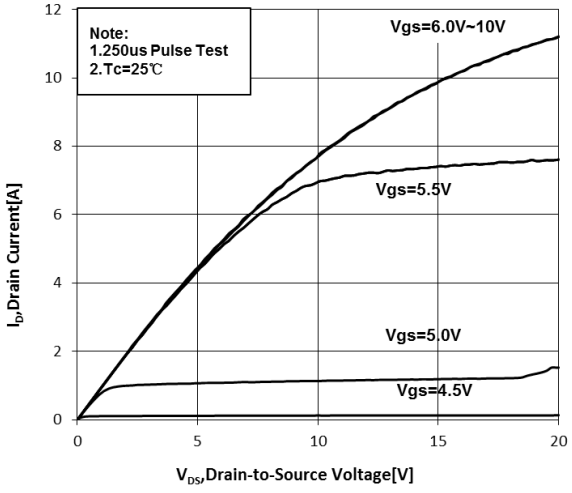


Figure 4 Typical Output Characteristics

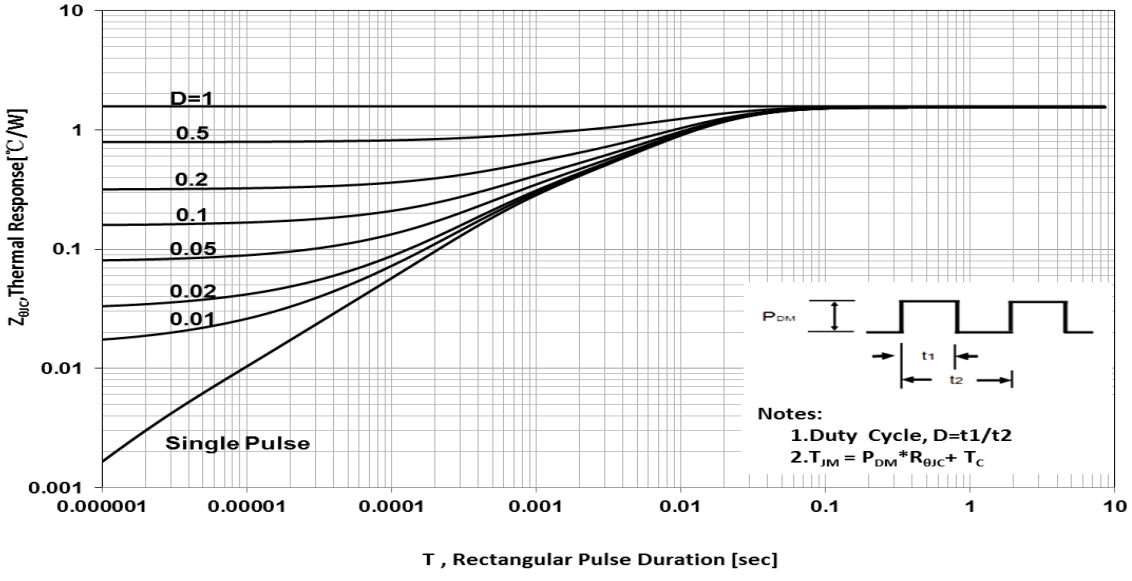
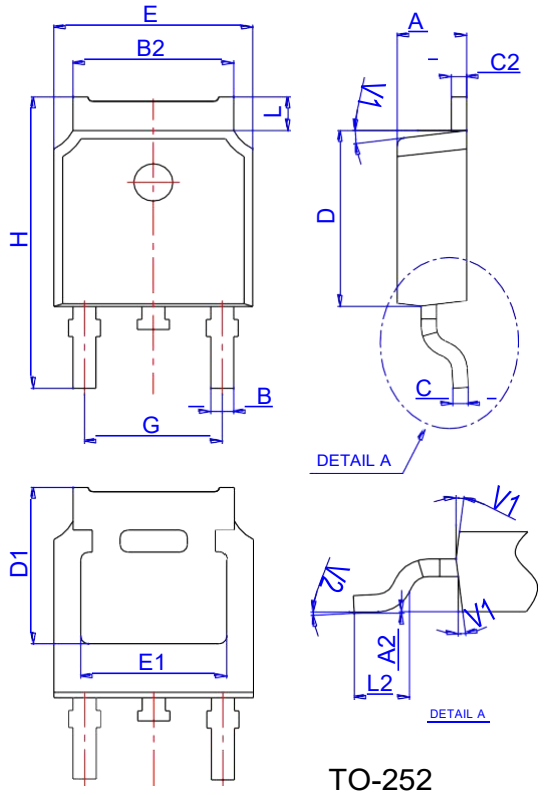


Figure 5 Maximum Effective Thermal Impedance , Junction to Case

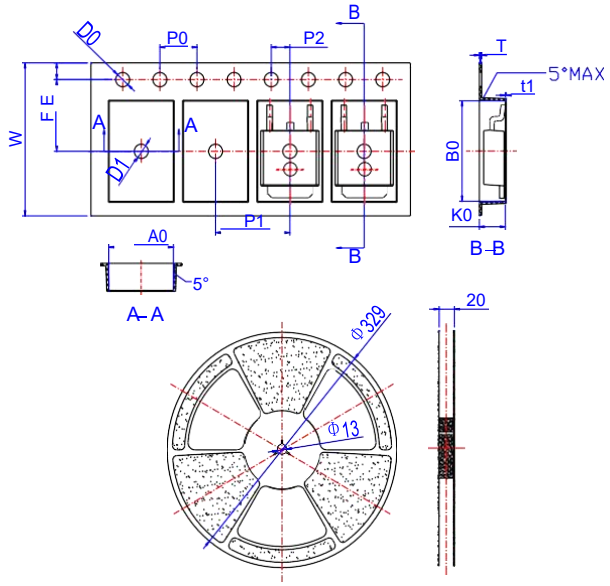
Package Mechanical Data-TO-252-JQ Single



TO-252

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583