General Description

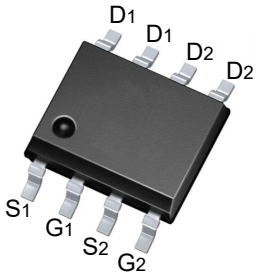
The MY7G04Cuses Trench Power LV MOSFET technology,High density cell design for low RDS(ON),.This deviceis suitable for use as a Battery protection or High Speed switching.

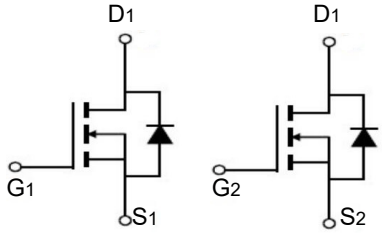
Features

V_{DSS}	40	-40	V
I_D	7	-7	A
$R_{DS(ON)}$(atV_{GS}=10V)	<37		mΩ
$R_{DS(ON)}$(atV_{GS}=4.5V)	<45		mΩ
$R_{DS(ON)}$(atV_{GS}=10V)	<-48		mΩ
$R_{DS(ON)}$(atV_{GS}=4.5V)	<-68		mΩ

Applications

- Power management
- Load switch
- Wireless charger





Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY7G04C	SOP-8	7G04C	3000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-source Voltage	V_{DS}	40	-40	V
Gate-source Voltage	V_{GS}	±20	±20	V
Drain Current	I_D	7	-7	A
Pulsed Drain Current [A]	I_{DM}	35	-30	A
Total Power Dissipation	P_D	2	2	W
Thermal Resistance Junction-to-Ambient [B]	$R_{\theta JA}$	62.5	62.5	℃/ W
Junction and Storage Temperature Range	T_J ,T_{STG}	-55～+150	-55～+150	℃

N-Channel Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V,V_{GS}=0V			1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1	1.5	3	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=7A			37	mΩ
		V_{GS}=4.5V, I_D=6A			45	
Diode Forward Voltage	V_{SD}	I_S=6A,V_{GS}=0V			1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=20V,V_{GS}=0V,f=1MHZ		381		pF
Output Capacitance	C_{oss}			50		
Reverse Transfer Capacitance	C_{rss}			15		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V,V_{DS}=20V,I_D=8A		10.3		nC
Gate-Source Charge	Q_{gs}			1.8		
Gate-Drain Charge	Q_{gd}			2.3		
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=20V, R_L=2.5Ω R_{GEN}=3Ω		4		ns
Turn-on Rise Time	t_r			18		
Turn-off Delay Time	$t_{D(off)}$			14		
Turn-off fall Time	t_f			20		

A. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.
B. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

P-Channel Electrical Characteristics (TJ=25 ℃, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-40			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-40V,V_{GS}=0V			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250μA	-1	-1.5	-3	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-7A		37	48	mΩ
		V_{GS}=-4.5V, I_D=-3.5A		58	68	
Diode Forward Voltage	V_{SD}	I_S=-4.2A,V_{GS}=0V			-1.2	V
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=-20V,V_{GS}=0V,f=1MHZ		522		pF
Output Capacitance	C_{oss}			103		
Reverse Transfer Capacitance	C_{rss}			64		
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=-10V,V_{DS}=-20V,I_D=-8A		13.3		nC
Gate-Source Charge	Q_{gs}			4.1		
Gate-Drain Charge	Q_{gd}			3.4		
Turn-on Delay Time	$t_{D(on)}$	V_{GEN}=-10V, V_{DD}=-20V, R_G=6Ω, R_L=2.3Ω		7.4		ns
Turn-on Rise Time	t_r			5.7		
Turn-off Delay Time	$t_{D(off)}$			20		
Turn-off fall Time	t_f			7		

C. Pulse Test: Pulse Width≤300us,Duty cycle ≤2%.
D. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

N-Channel Typical Characteristics

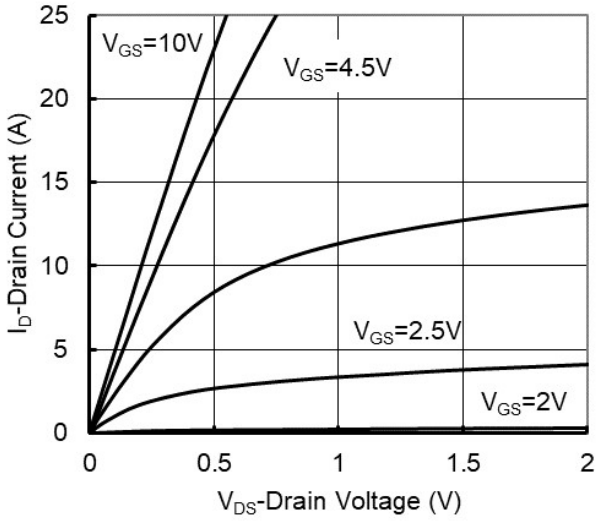


Figure1. Output Characteristics

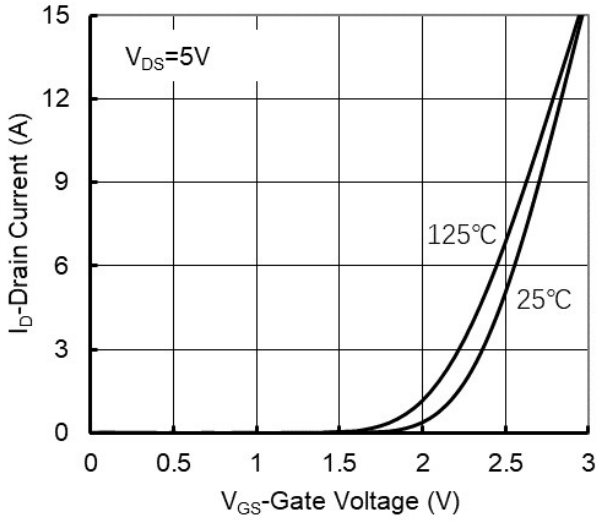


Figure2. Transfer Characteristics

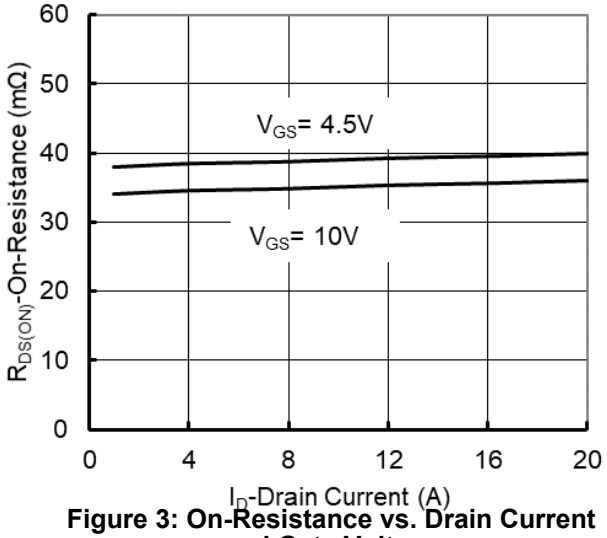


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

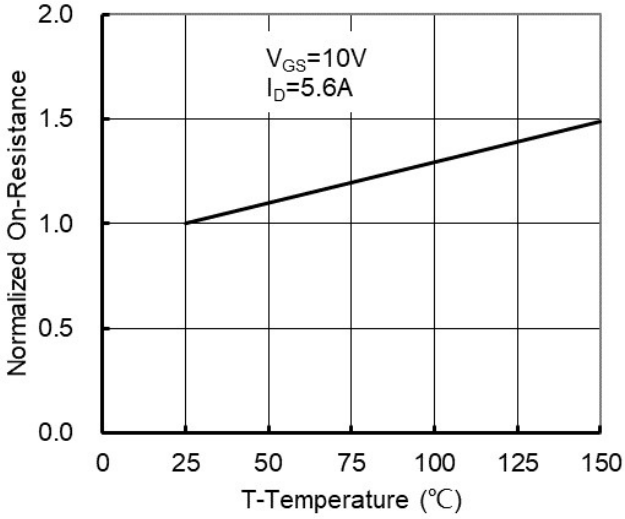


Figure 4: On-Resistance vs. Junction Temperature

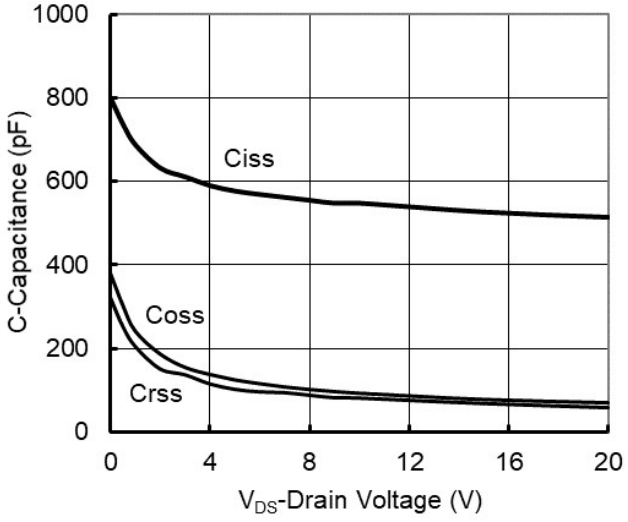


Figure5. Capacitance Characteristics

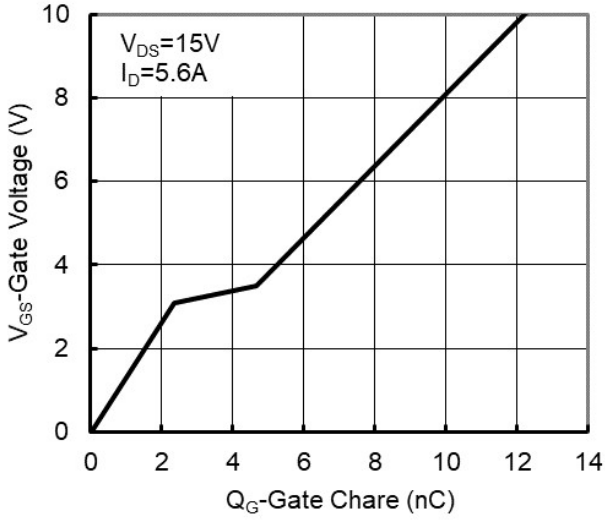


Figure6. Gate Charge

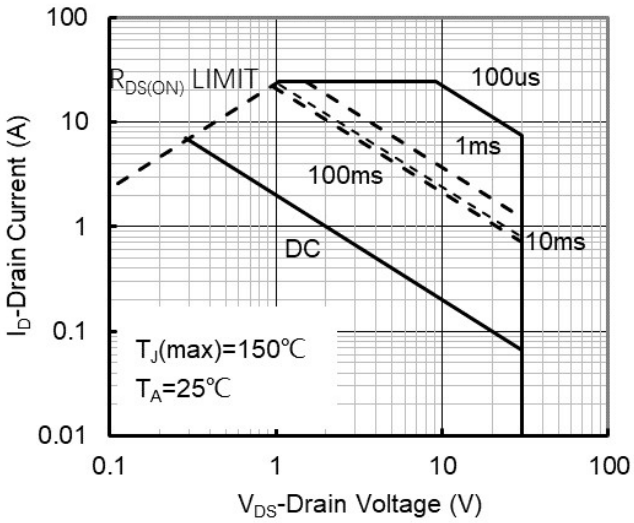


Figure7. Safe Operation Area

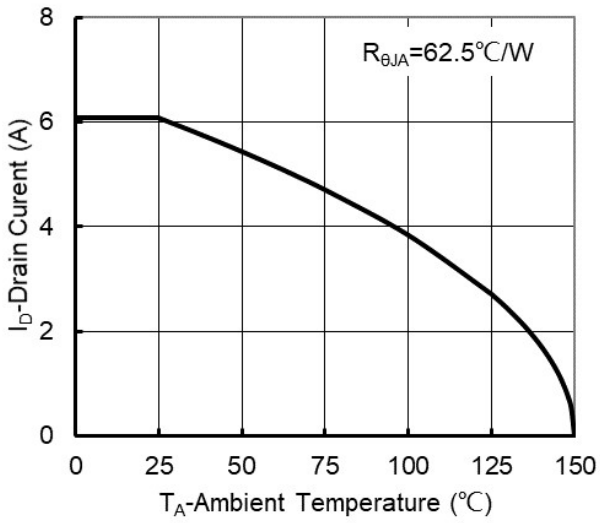


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

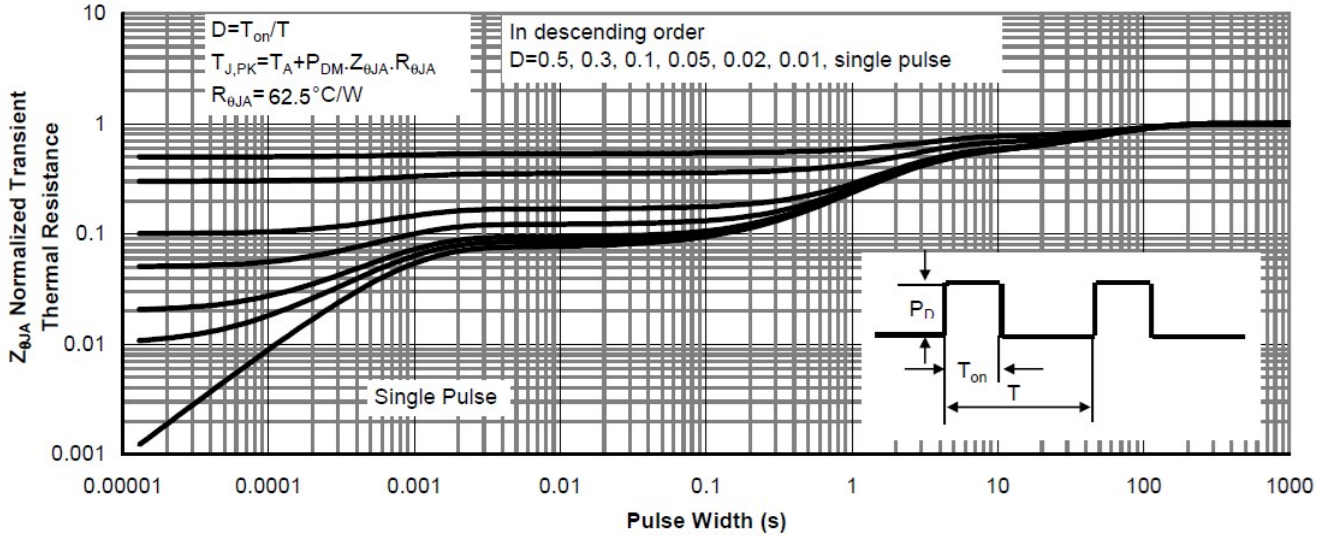


Figure9.Normalized Maximum Transient Thermal Impedance

P-Channel Typical Characteristics

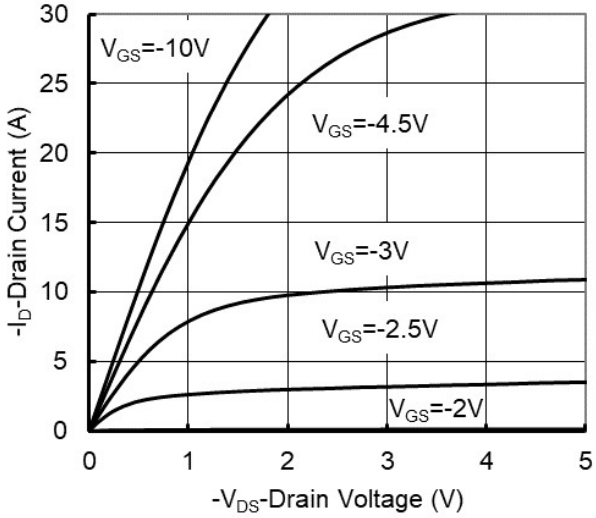


Figure1. Output Characteristics

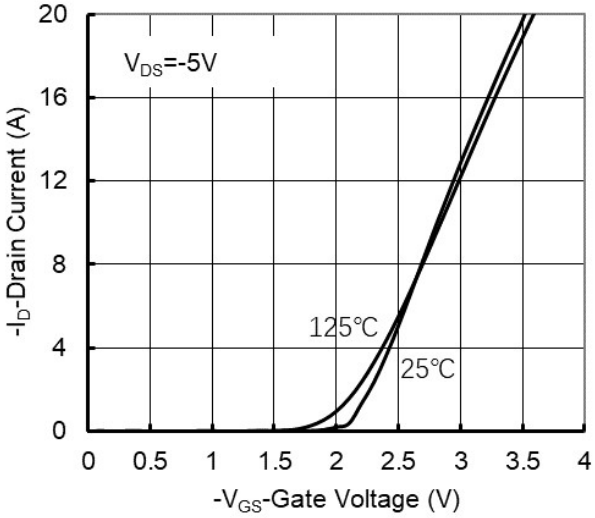


Figure2. Transfer Characteristics

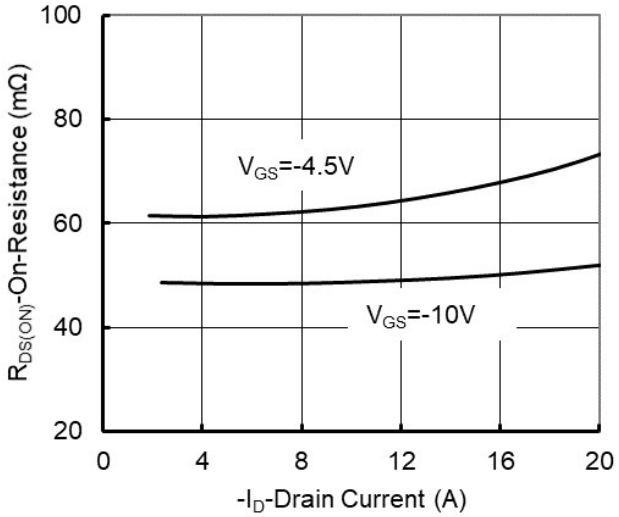


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

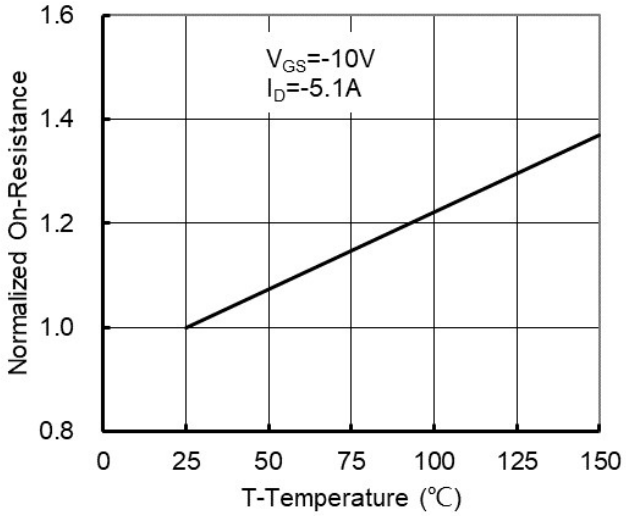


Figure 4: On-Resistance vs. Junction Temperature

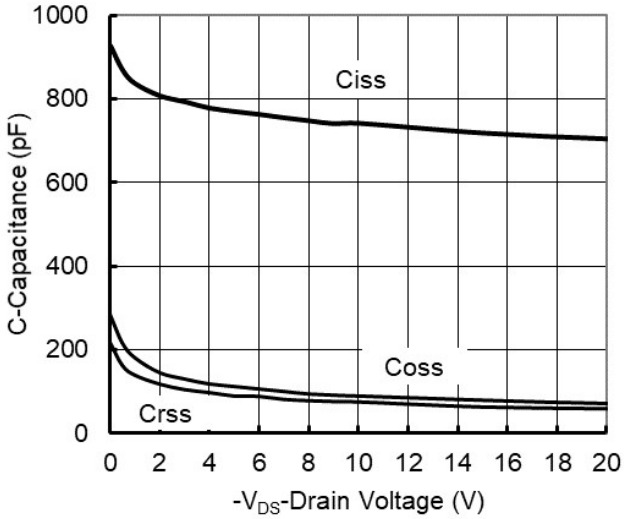


Figure5. Capacitance Characteristics

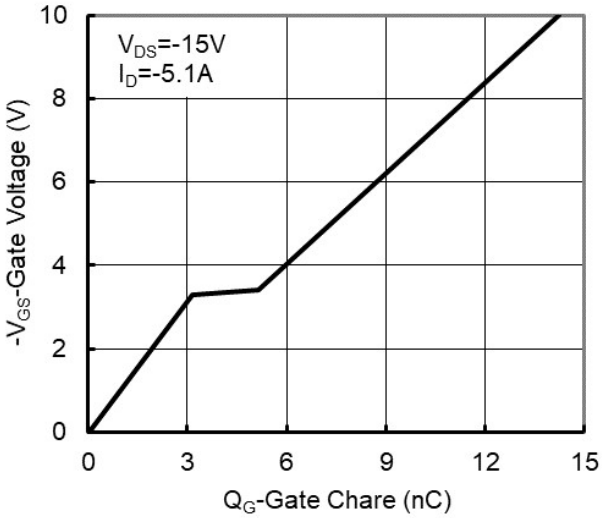


Figure6. Gate Charge

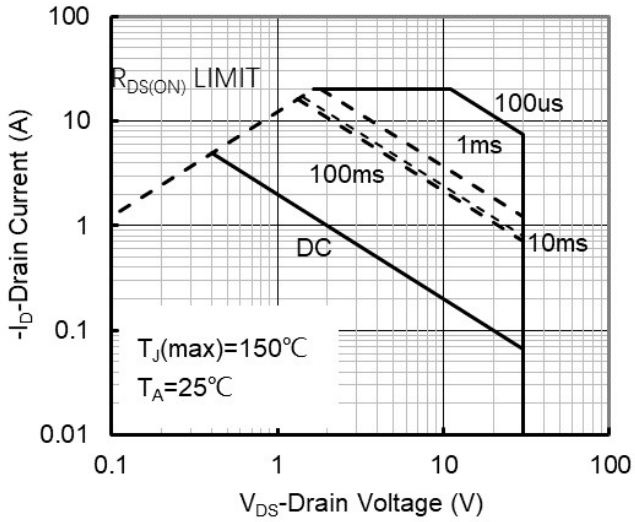


Figure7. Safe Operation Area

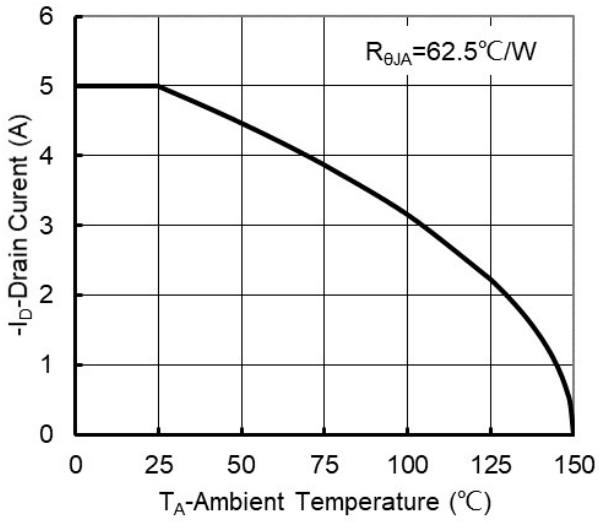


Figure8. Maximum Continuous Drain Current vs Ambient Temperature

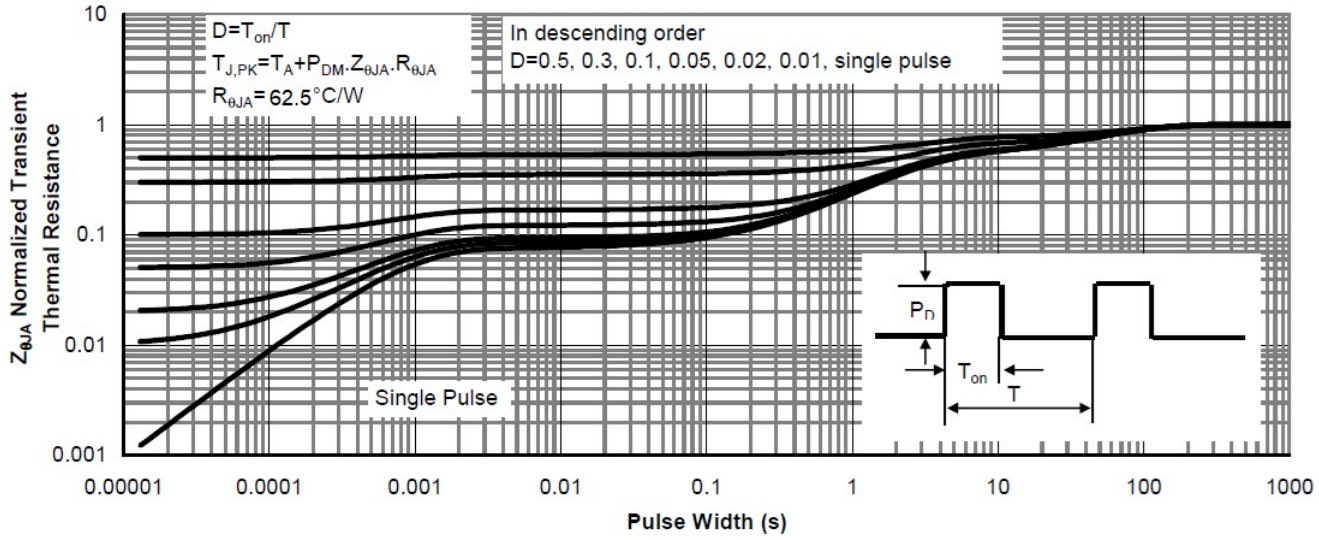
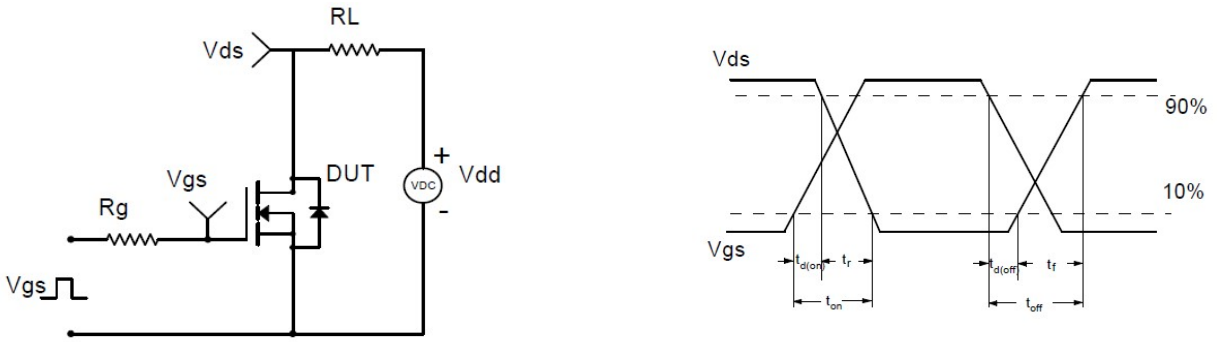
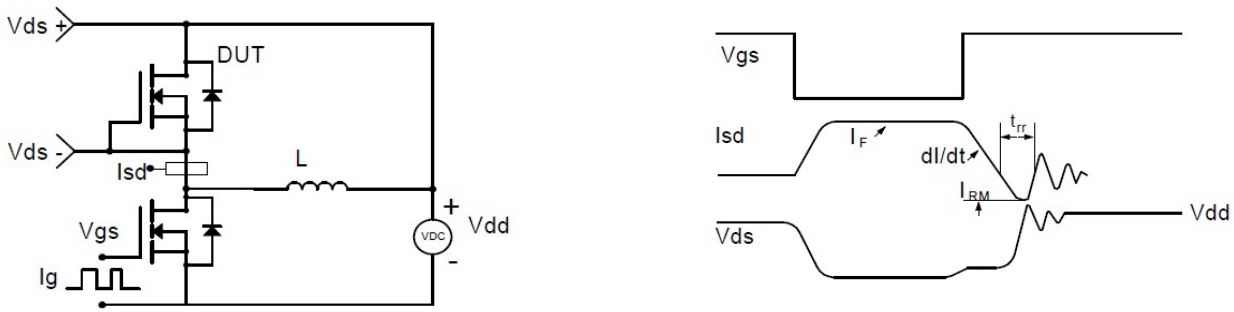


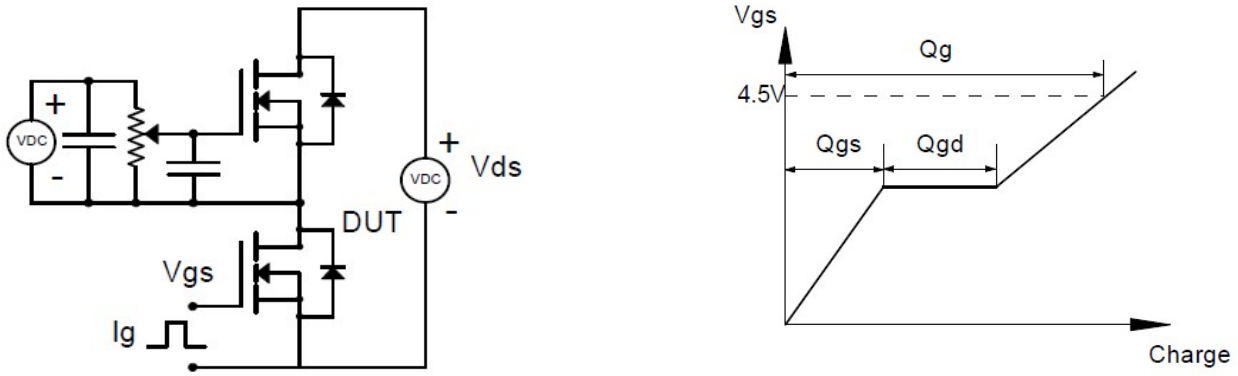
Figure9.Normalized Maximum Transient Thermal Impedance



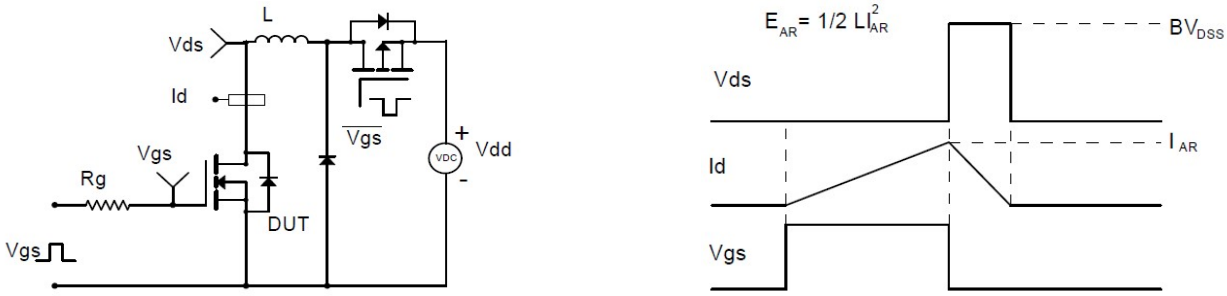
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

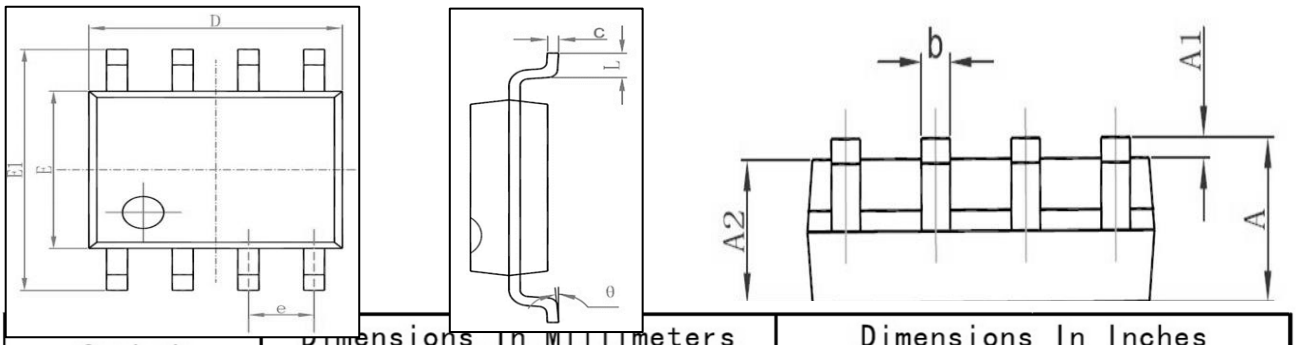


Gate Charge Test Circuit & Waveform

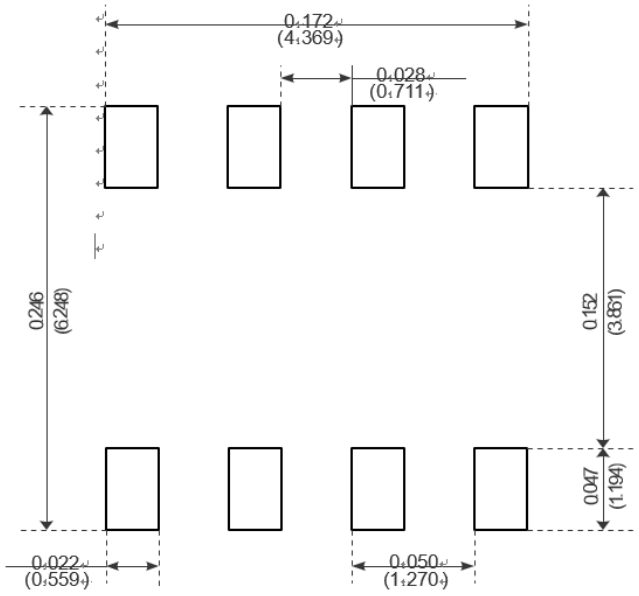


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

Package Mechanical Data-SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



Recommended Minimum Pads