MY75N75P

75V N-Channel Enhancement Mode MOSFET

MAOYUANWEI semiconductor

General Description

The MY75N75P is silicon N-channel Enhanced VDMOSFETS, obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy.

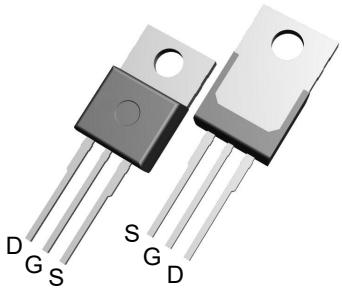
RoHS Compliant

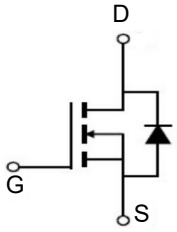
Features

V_{DSS}	75	V
I_D	75	A
$R_{DS(ON)}$(atV_{GS} = 4.5V)	< 8	mΩ
$R_{DS(ON)}$(atV_{GS} = 10V)	< 12	mΩ

Application

- High efficiency switch mode power supplies
- Power factor correction
- Electronic lamp ballast





Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY75N75P	TO-220	MY75N75P	1000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	75	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [G]	T_C=25°C	I_D	80	A
	T_C=100°C		75	
Pulsed Drain Current [C]		I_{DM}	245	
Continuous Drain Current	T_A=25°C	I_{DSM}	13	A
	T_A=70°C		10.5	
Avalanche Current [C]		I_{AS}	50	A
Avalanche energy L=0.1mH [C]		E_{AS}	125	mJ
Power Dissipation [B]	T_C=25°C	P_D	167	W
	T_C=100°C		83	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2.1	W
	T_A=70°C		1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Electrical Characteristics (T_C=25 ℃, unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	75			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V, V_{GS}=0V			1	
		T_J=55°C			5	μA
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	2	3	4	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	245			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		7	8	mΩ
		TO220 T_J=125°C		10	12	mΩ
		V_{GS}=6V, I_D=20A TO-220		6.1	7.9	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		60		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current [G]				70	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=40V, f=1MHz		3142		pF
C_{oss}	Output Capacitance			435		pF
C_{rss}	Reverse Transfer Capacitance			43		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.6	1.3	2.0	Ω
SWITCHING PARAMETERS						
$Q_{g(10V)}$	Total Gate Charge	V_{GS}=10V, V_{DS}=40V, I_D=20A		44.5	63	nC
Q_{gs}	Gate Source Charge			12		nC
Q_{gd}	Gate Drain Charge			8		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=40V, R_L=2Ω, R_{GEN}=3Ω		13.5		ns
t_r	Turn-On Rise Time			11		ns
$t_{D(off)}$	Turn-Off DelayTime			32		ns
t_f	Turn-Off Fall Time			11		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/μs		29		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/μs		161		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25 ℃. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150 ℃. The value in any given application depends on the user's specific board design, and the maximum temperature of 175 ℃ may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175 ℃, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175 ℃. Ratings are based on low frequency and duty cycles to keep initial T_J =25 ℃.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175 ℃. The SOA curve provides a single pulse rating.

G. The maximum current limited by package.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25 ℃.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

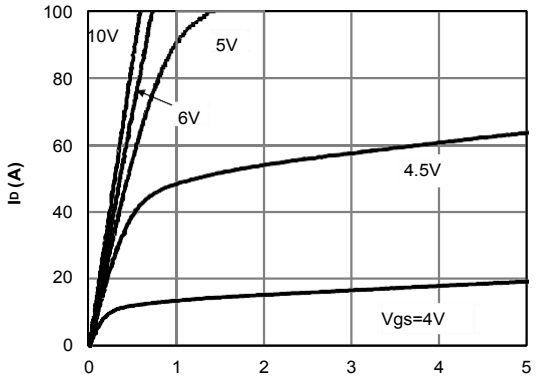


Fig 1: On-Region Characteristics (Note E)

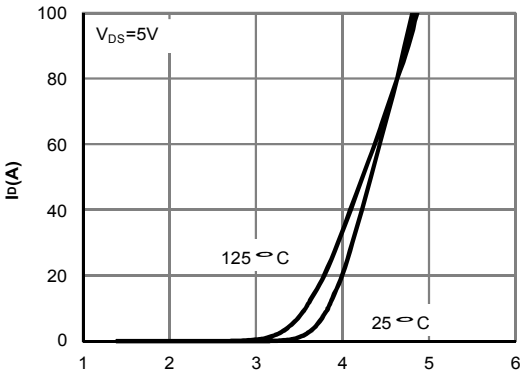


Figure 2: Transfer Characteristics (Note E)

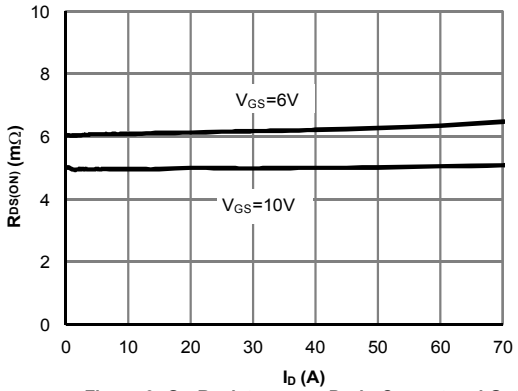


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

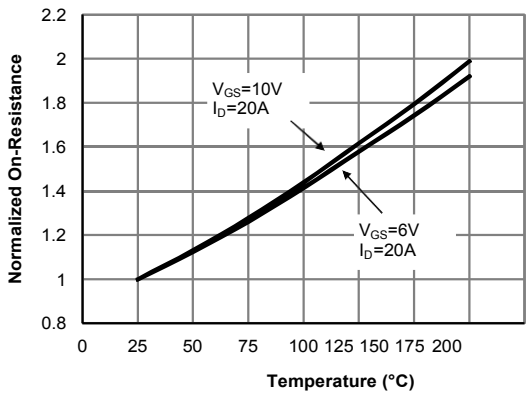


Figure 4: On-Resistance vs. Junction Temperature (Note E)

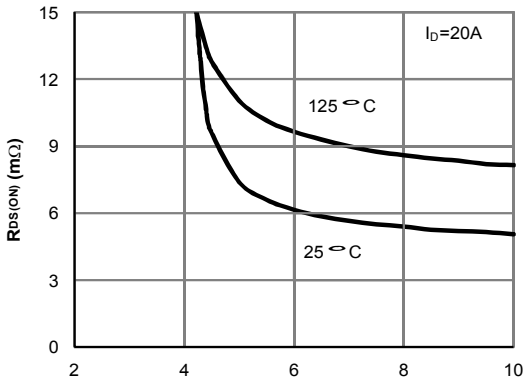


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

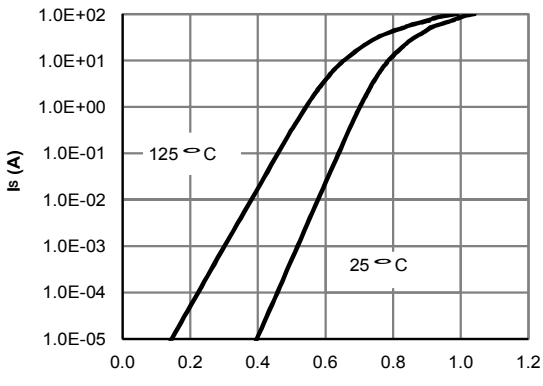


Figure 6: Body-Diode Characteristics (Note E)

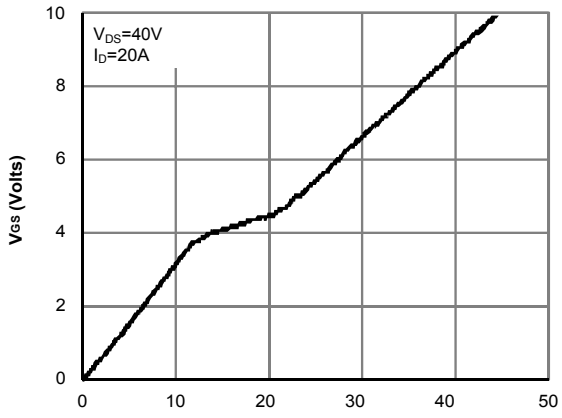


Figure 7: Gate-Charge Characteristics

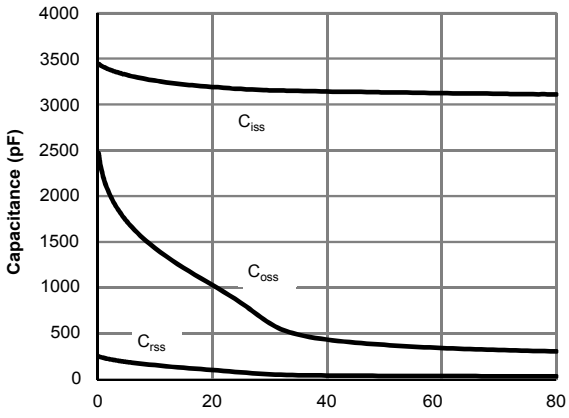


Figure 8: Capacitance Characteristics

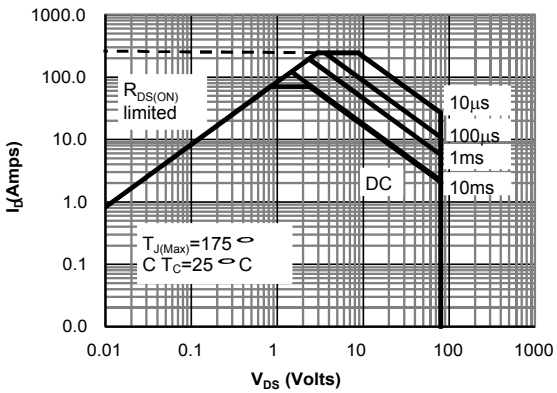


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

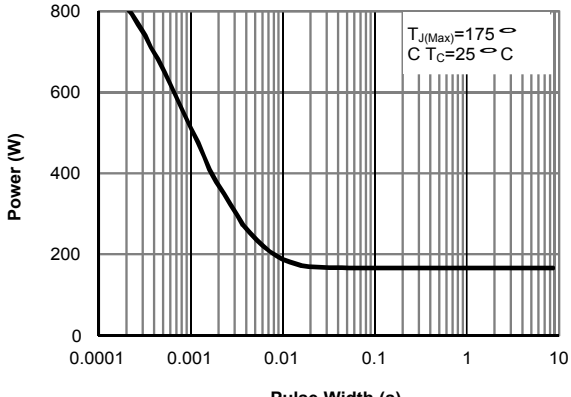


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

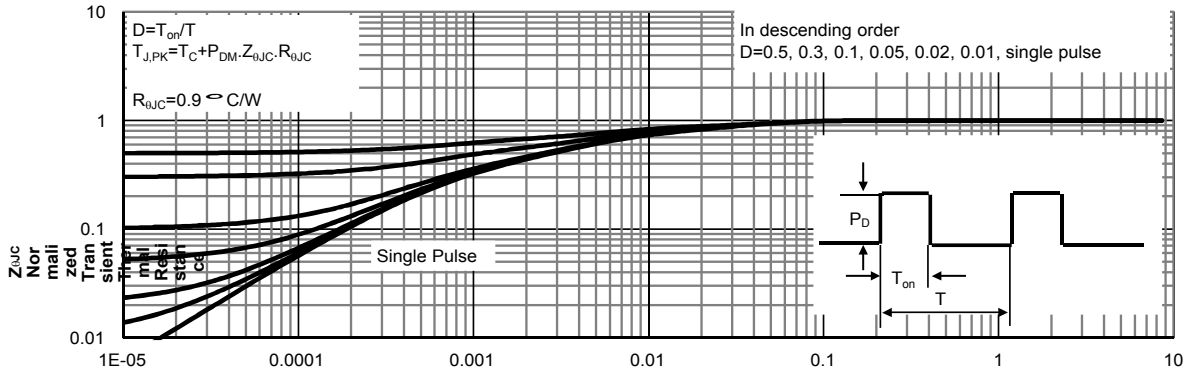


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

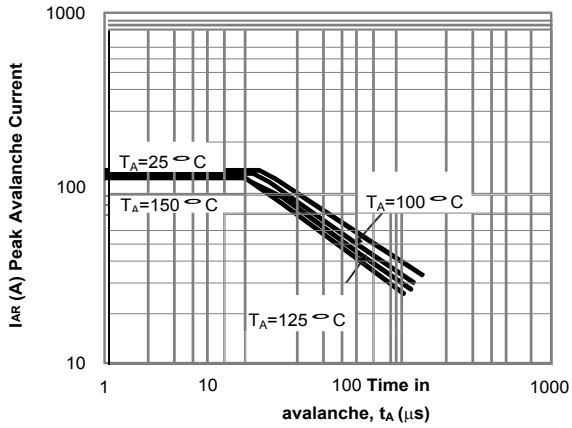


Figure 12: Single Pulse Avalanche capability (Note C)

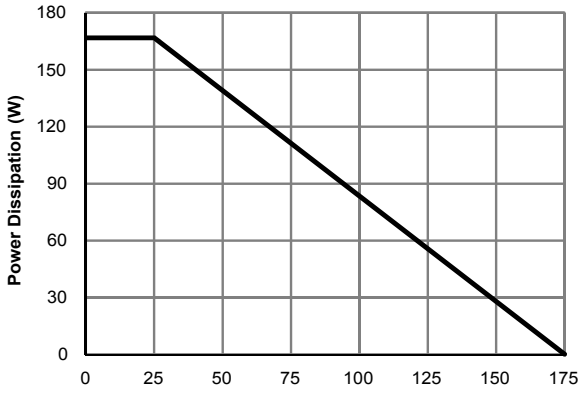


Figure 13: Power De-rating (Note F)

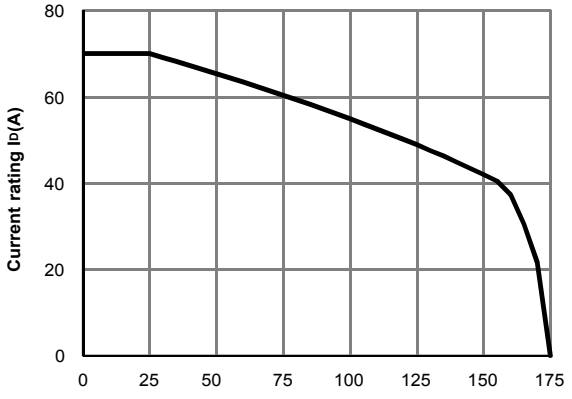


Figure 14: Current De-rating (Note F)

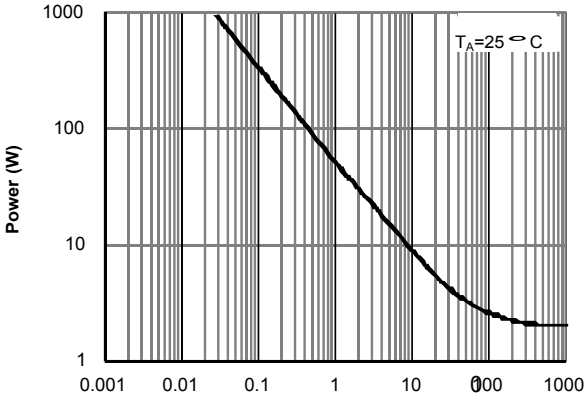


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

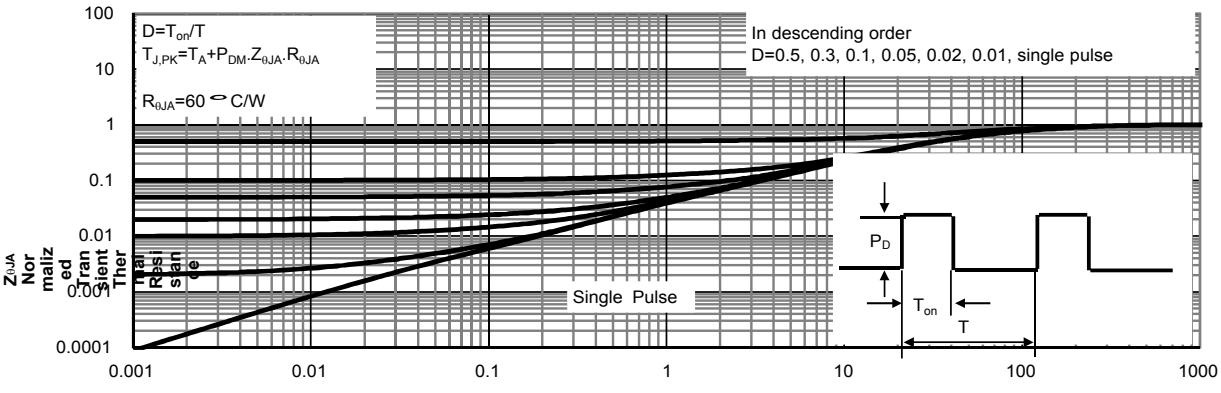
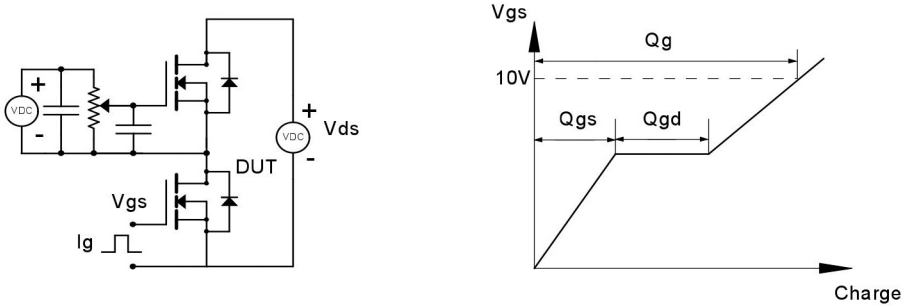
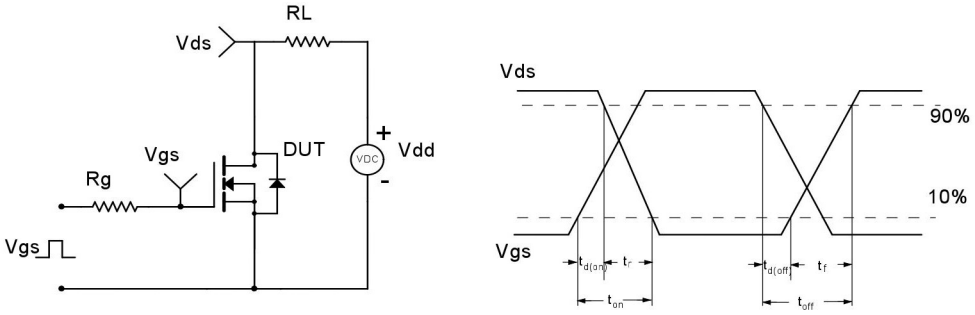


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

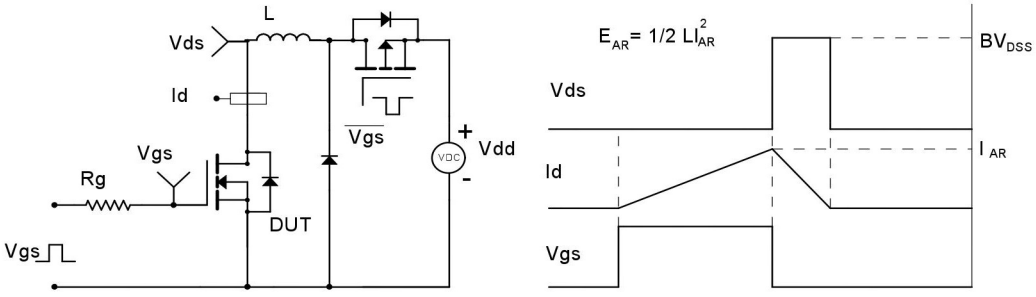
Gate Charge Test Circuit & Waveform



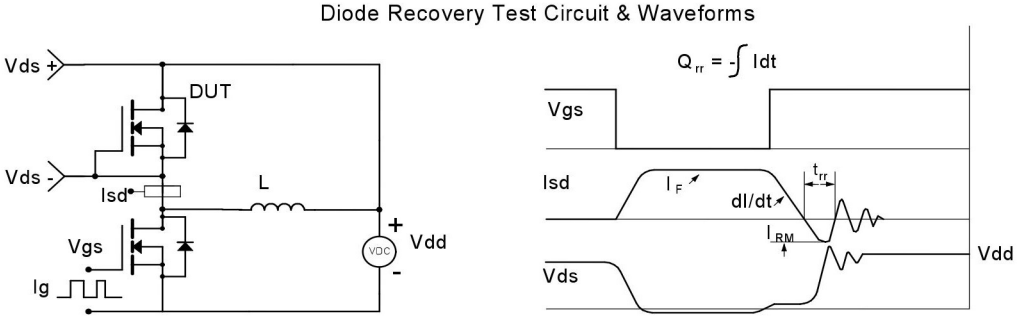
Resistive Switching Test Circuit & Waveforms



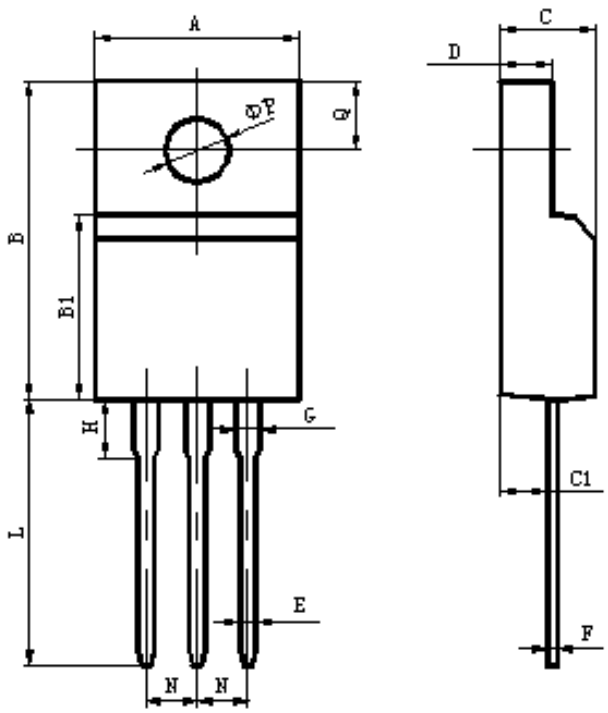
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Mechanical Data-TO-220 Single



Items	Values(mm)	
	MIN	MAX
A	9.60	10.4
B	15.4	16.2
B1	8.90	9.50
C	4.30	4.90
C1	2.10	3.00
D	2.40	3.00
E	0.60	1.00
F	0.30	0.60
G	1.12	1.42
H	3.40	3.80
	2.40	2.90
L*	12.0	14.0
N	2.34	2.74
Q	3.15	3.55
Φ P	2.90	3.30