MY70N10C

100V N-SGT Enhancement Mode MOSFET

MAOYUANWEI semiconductor

General Description

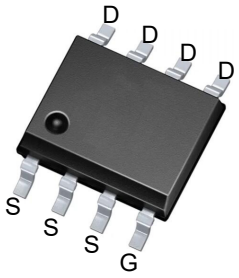
The MY70N10C use advanced SGT MOSFET technology to provide low RDS(ON), low gate charge, fast switching and excellent avalanche characteristics. This device is specially designed to get better ruggedness and suitable to use in

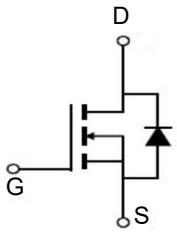
Features

V_{DSS}	100	V
I_D	80	A
$R_{DS(ON)}$(atV_{GS}=10V)	6.4	mΩ
$R_{DS(ON)}$(atV_{GS}=4.5V)	9.3	mΩ

Application

- Battery protection
- Load switch
- Uninterruptible power supply





Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY70N10C	SOP-8	MY70N10C	3000

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain source voltage	VDS	100	V
Gate source voltage	VGS	±20	V
Continuous drain current[1], T_C=25 ℃	ID	68	A
Pulsed drain current[2], T_C=25 ℃	ID, pulse	180	A
Power dissipation[3], T_C=25 ℃	P_D	125	W
Single pulsed avalanche energy[5]	EAS	100	mJ
Operation and storage temperature	Tstg , Tj	-55 to 150	℃
Thermal resistance, junction-case	RθJC	1	℃/W
Thermal resistance, junction-ambient[4]	RθJA	62	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Parameter	Symbol	Test condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0 V, I_D=250 μA	100			V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS} , I_D=250 μA	1.2	2.0	2.5	V
Drain-source on-state resistance	$R_{DS(ON)}$	V_{GS}=10 V, I_D=20 A		6.4	7.7	mΩ
Drain-source on-state resistance	$R_{DS(ON)}$	V_{GS}=4.5 V, I_D=15 A		9.3	11.6	mΩ
Gate-source leakage current	I_{GSS}	V_{GS}=20 V			100	nA
					-100	
Drain-source leakage current	I_{DSS}	V_{DS}=100 V, V_{GS}=0 V			1	μA
Input capacitance	Ciss	V_{GS}=0 V, V_{DS}=50 V, f=1 MHz		2604		pF
Output capacitance	Coss			361.2		pF
Reverse transfer capacitance	Crss			6.5		pF
Turn-on delay time	td(on)	V_{GS}=10 V, V_{DS}=50 V, R_G=2.2 Ω, I_D=25 A		20.6		ns
Rise time	t_r			5		ns
Turn-off delay time	td(off)			51.8		ns
Fall time	t_f			9		ns
Total gate charge	Q_g	I_D=25A, V_{DS}=50 V, V_{GS}=10 V		49.9		nC
Gate-source charge	Q_{gs}			6.5		nC
Gate-drain charge	Q_{gd}			12.4		nC
Gate plateau voltage	$V_{plateau}$			3.4		V
Diode forward current	I_S	V_{GS}<V_{th}			60	
Pulsed source current	I_{SP}				180	A
Diode forward voltage	V_{SD}	I_S=12 A, V_{GS}=0 V			1.3	V
Reverse recovery time	t_{rr}	I_S=12 A, di/dt=100 A/μs		60.2		ns
Reverse recovery charge	Q_{rr}			106.1		nC
Peak reverse recovery current	I_{rrm}			3		A

Note

1) Calculated continuous current based on maximum allowable junction temperature.
2) Repetitive rating; pulse width limited by max. junction temperature.
3) Pd is based on max. junction temperature, using junction-case thermal resistance.
4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_a=25 ℃ .
5) V_{DD}=50 V, R_G=25 Ω, L=0.3 mH, starting T_j=25 ℃ .

Typical Characteristics

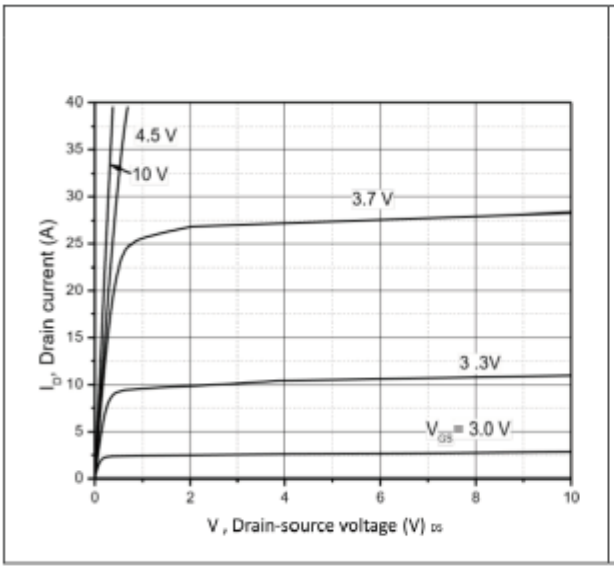


Figure 1, Typ. output characteristics

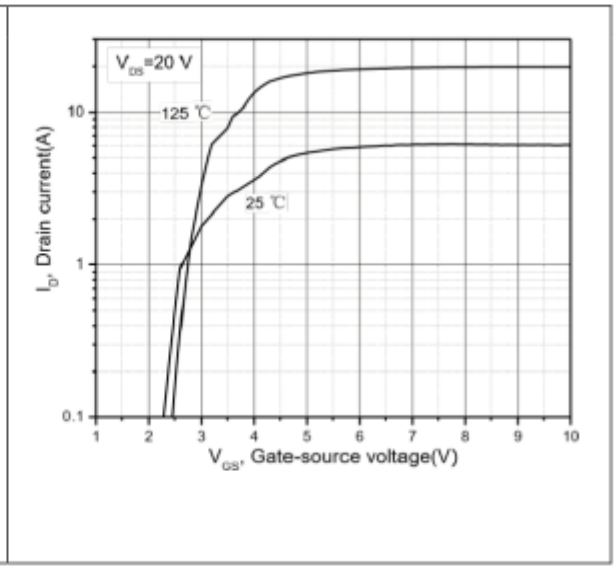


Figure 2, Typ. transfer characteristics

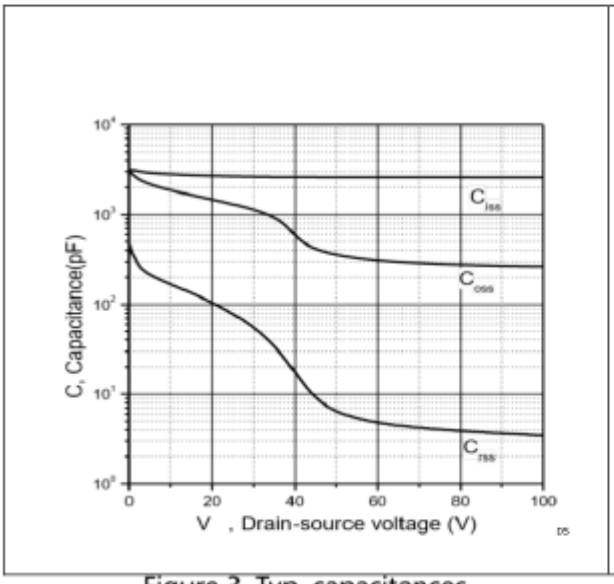


Figure 3, Typ. capacitances

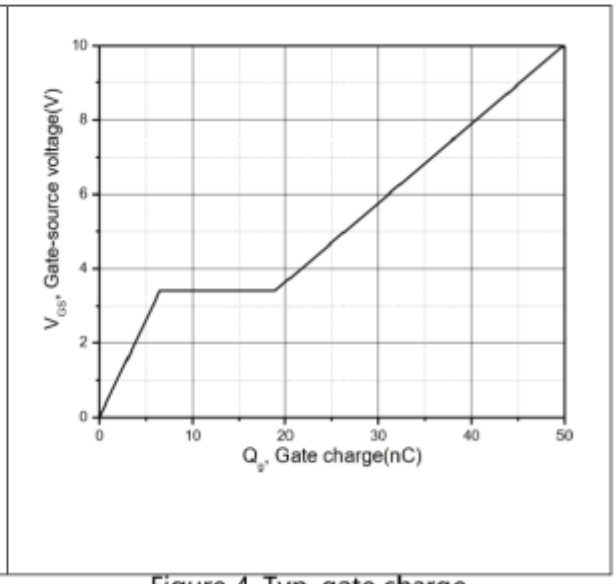


Figure 4, Typ. gate charge

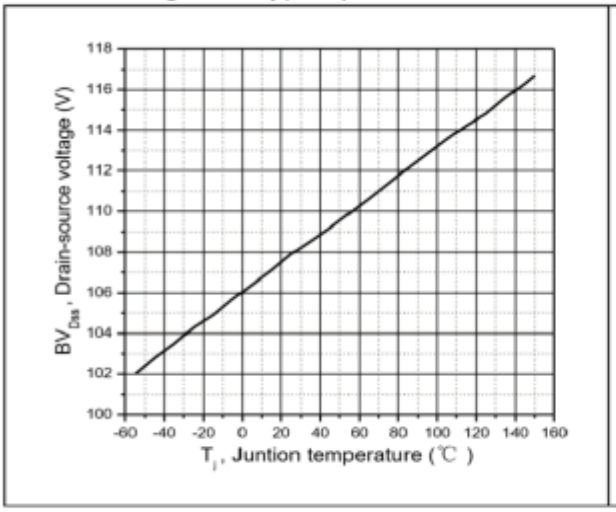


Figure 5, Drain-source breakdown voltage

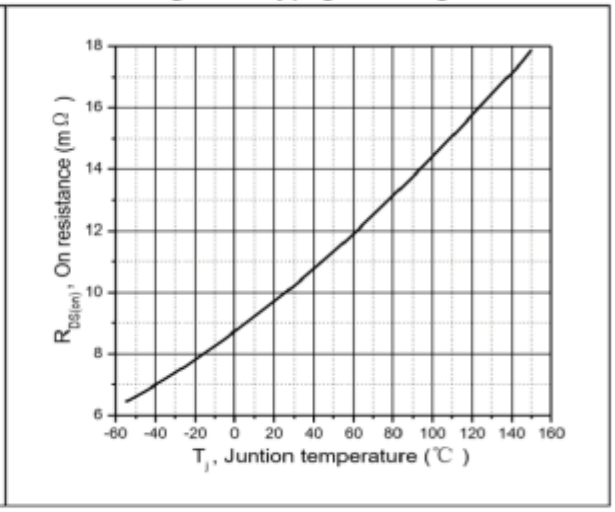


Figure 6, Drain-source on-state resistance

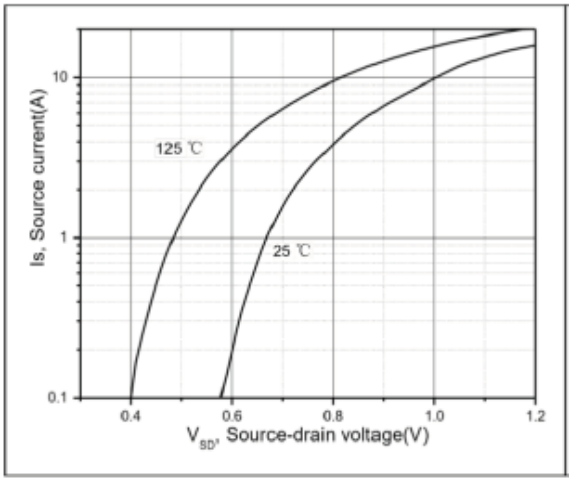


Figure 7, Forward characteristic of body diode

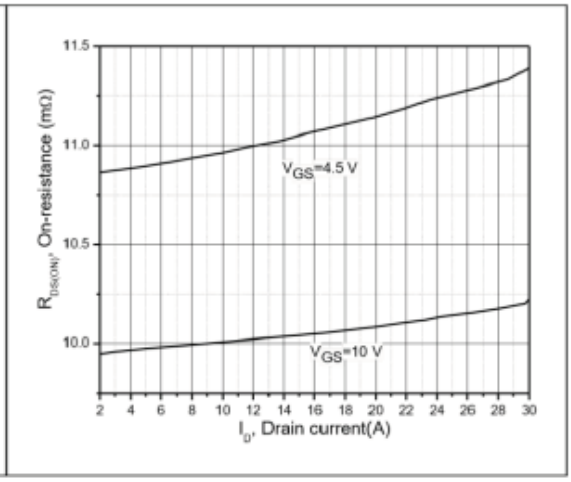


Figure 8, Drain-source on-state resistance

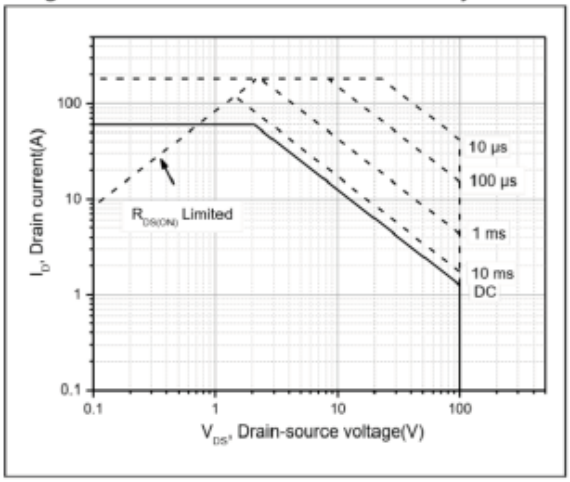


Figure 9, Safe operation area T_C=25 ℃

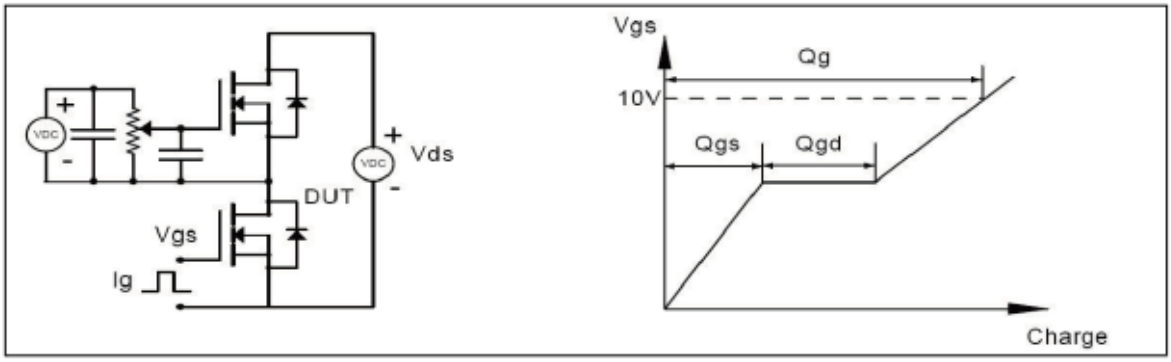


Figure 1, Gate charge test circuit & waveform

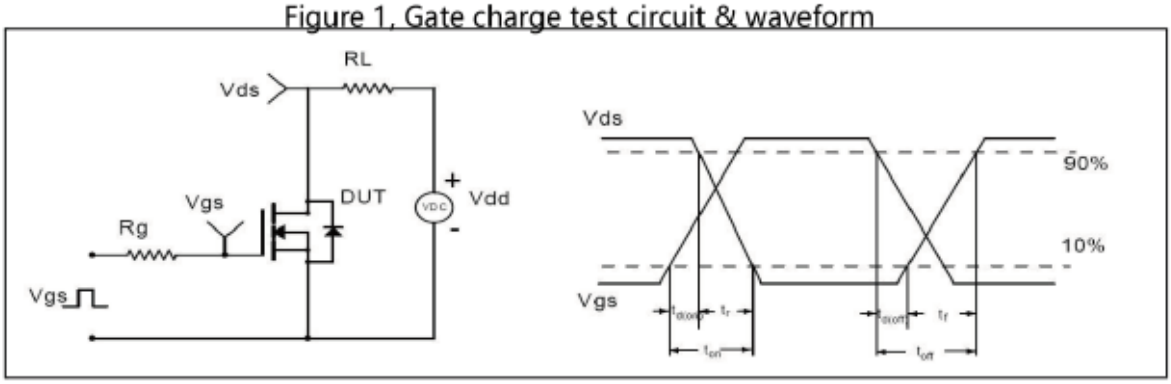


Figure 2, Switching time test circuit & waveforms

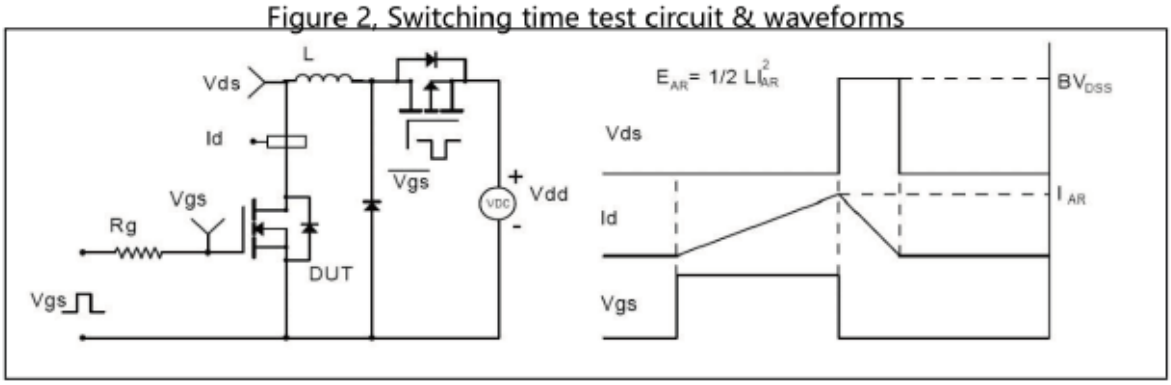


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

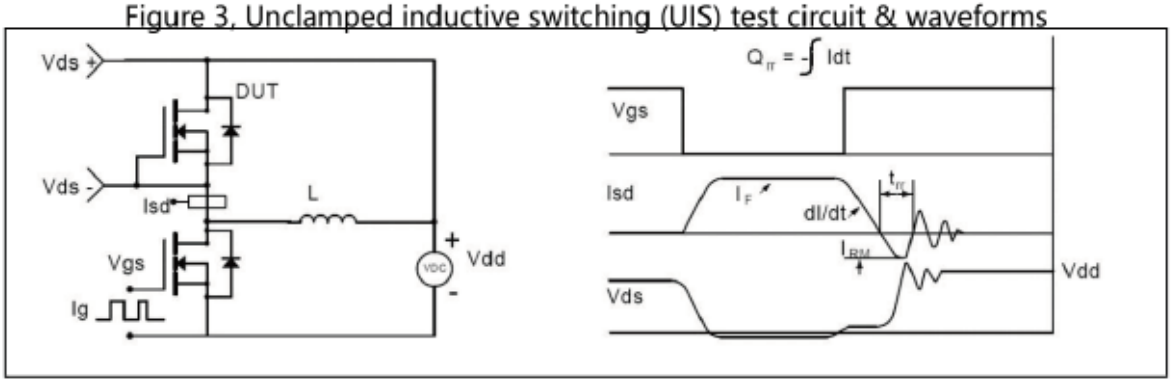
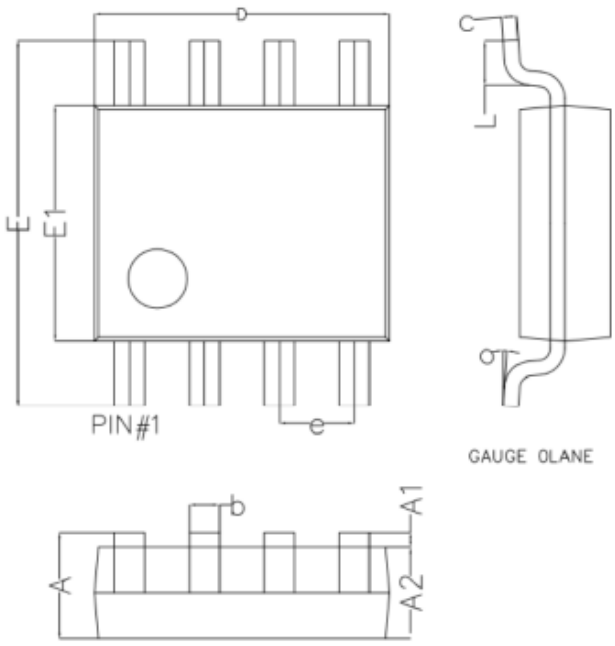


Figure 4, Diode reverse recovery test circuit & waveforms

Package Mechanical Data-SOP-8-JQ Single



Symbol	Dim in mm		
	Min	Nor	Max
A	1.350	1.550	1.750
A1	0.100	0.175	0.250
A2	1.350	1.450	1.550
b	0.330	0.420	0.510
c	0.170	0.210	0.250
D	4.800	4.900	5.000
e	1.270(BSC)		
E	5.800	6.000	6.200
E1	3.800	3.900	4.000
L	0.400	0.835	1.2700
o	0°	4°	8°