MY65T180PT

650V N-Channel Enhancement Mode MOSFET

MAOYUANWEI semiconductor

General Description

The MY65T180PT is silicon N-channel Enhanced VDMOSFETs, obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy.

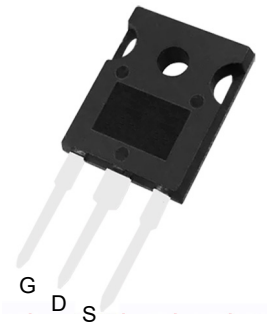
RoHS Compliant

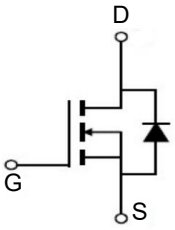
Features

V_{DSS}	650	V
I_D	20	A
P_D(T_C=25℃)	416	W
$R_{DS(ON)}$(atV_{GS} = 10V)	0.27	Ω

Application

- Fast Switching
- Low ON Resistance
- Low Gate Charge
- Power factor correction





Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY65T180PT	TO-247	MY65T180PT	600

Absolute Maximum Ratings (T_C=25℃unless otherwise noted)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		650	V
V_{GSS}	Gate-Source Voltage		±30	V
I_D	Continuous Drain Current	T_C = 25℃	20	A
		T_C = 100℃	13	A
I_{DM}	Pulsed Drain Current note1		80	A
E_{AS}	Single Pulsed Avalanche Energy note2		1350	mJ
P_D	Power Dissipation	T_C = 25℃	416	W
$R_{\theta JC}$	Thermal Resistance, Junction to Case		0.3	℃/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		60	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Electrical Characteristics (T_C=25 ℃, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V,I_D=250μA	650	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 600V, V_{GS} = 0V,T_J= 25℃	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	V_{DS}=0V, V_{GS} = ±30V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250μA	2	3	4	V
$R_{DS(on)}$	Static Drain-Source on-Resistance note3	V_{GS} =10V, I_D =10A	-	0.27	0.45	Ω
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1.0MHz	-	2980	-	pF
C_{oss}	Output Capacitance		-	291	-	pF
C_{rss}	Reverse Transfer Capacitance		-	40	-	pF
Q_g	Total Gate Charge	V_{DD} = 480V, I_D = 20A, V_{GS} = 10V	-	80	-	nC
Q_{gs}	Gate-Source Charge		-	12	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	34	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 250V, I_D =20A, R_G = 25Ω	-	37	-	ns
t_r	Turn-on Rise Time		-	66	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	175	-	ns
t_f	Turn-off Fall Time		-	84	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	20	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	80	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_{SD} = 20A	-	-	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} =0V, I_S=20A, di/dt=100A/μs	-	450	-	ns
Q_{rr}	Reverse Recovery Charge		-	7.1	-	μC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. I_{AS} =16A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤1%

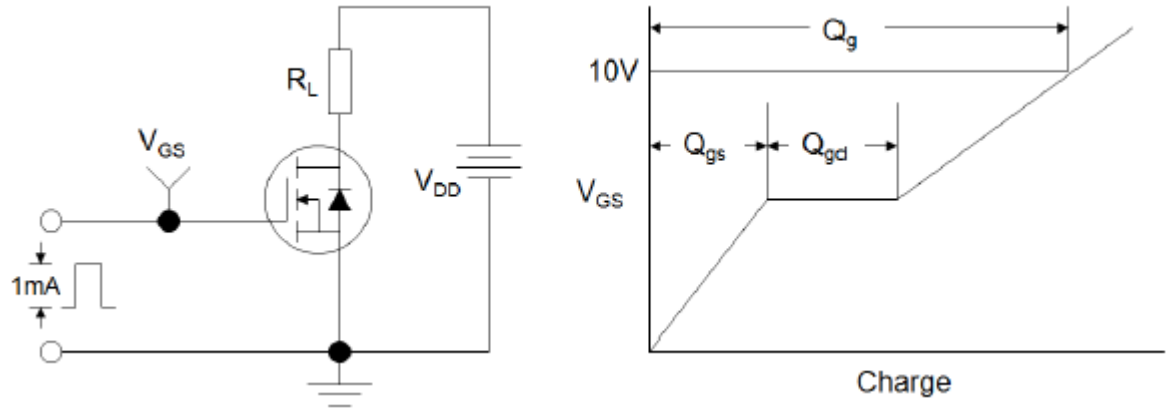


Figure1:Gate Charge Test Circuit & Waveform

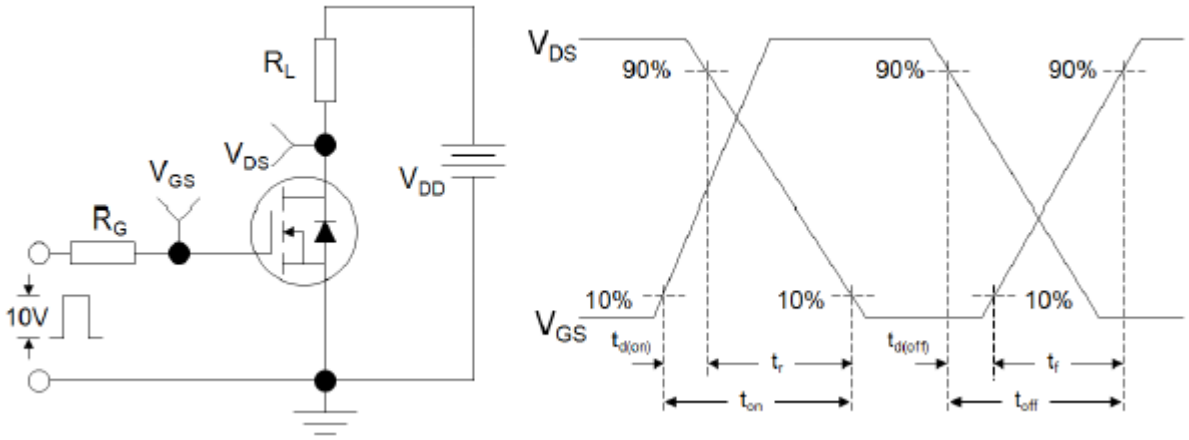


Figure 2: Resistive Switching Test Circuit & Waveforms

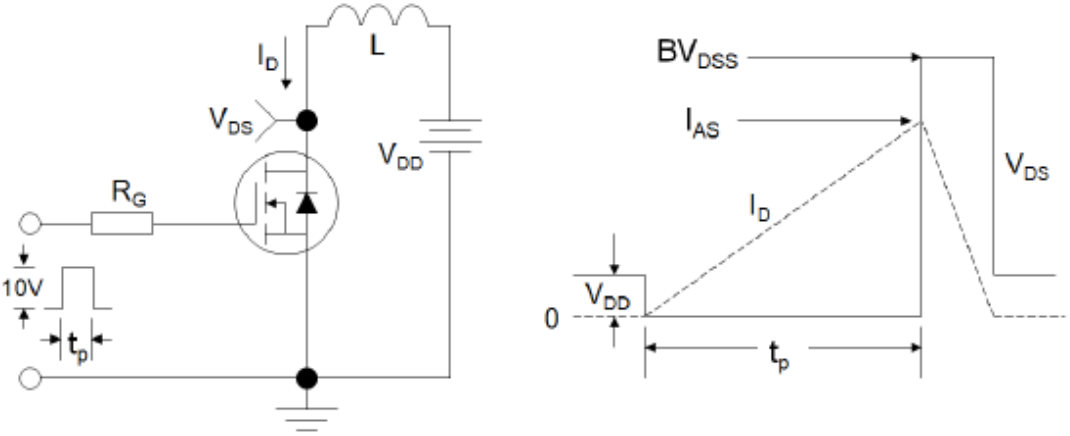


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

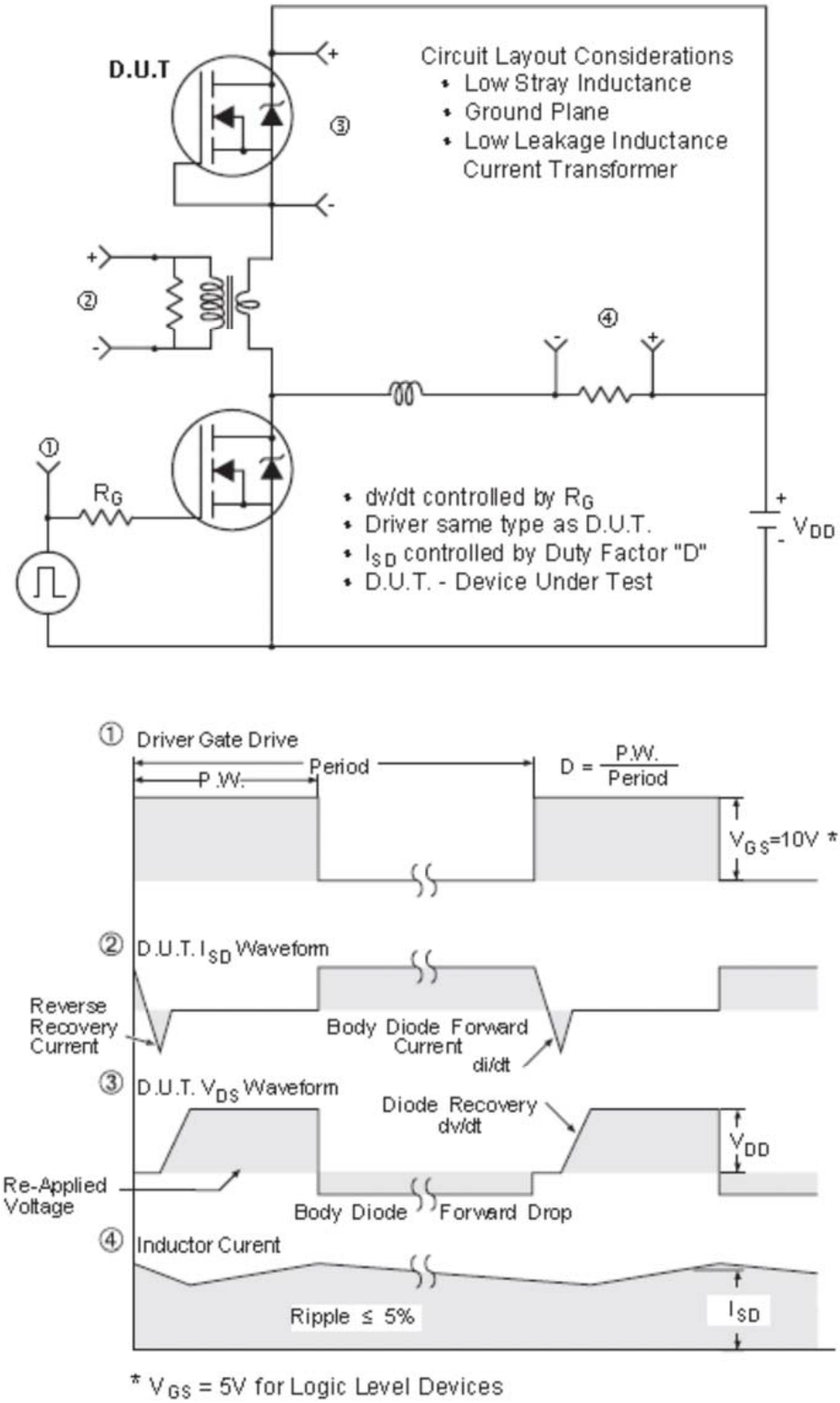
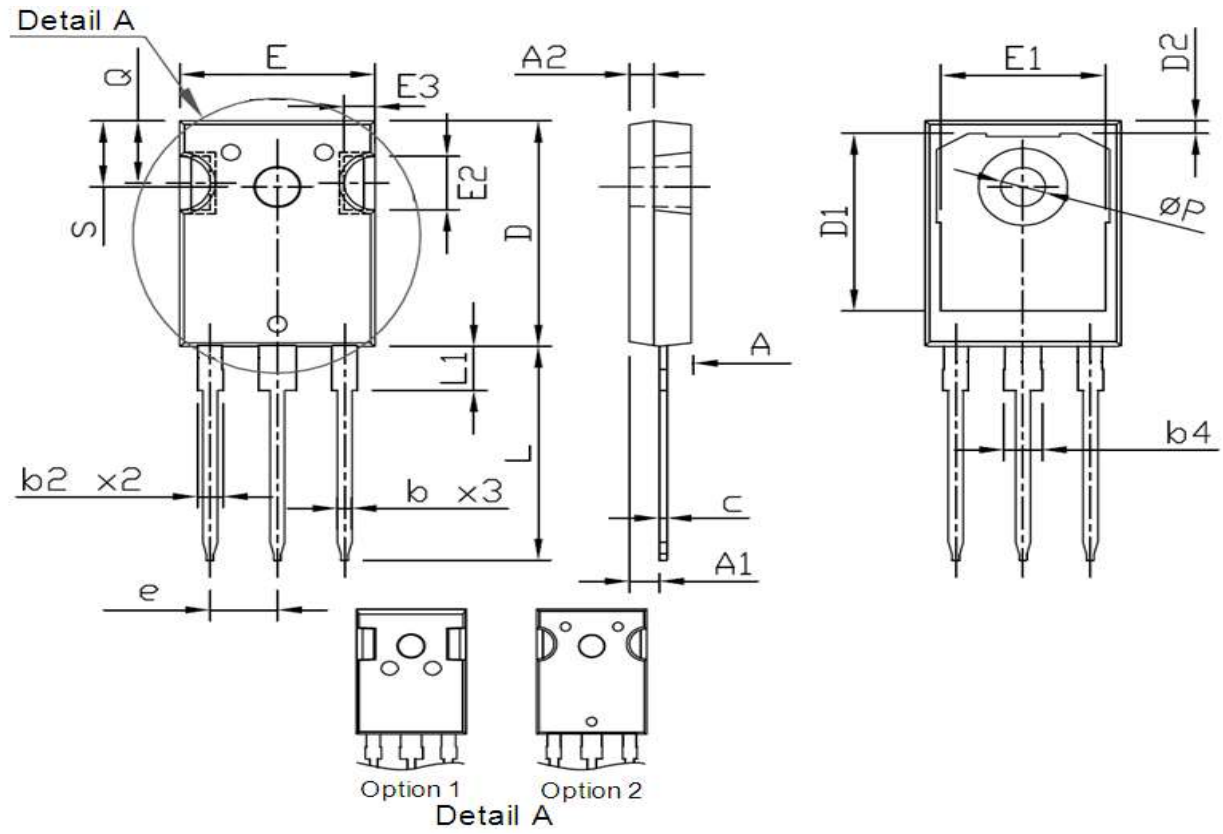


Figure 4:Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

Package Mechanical Data-TO-247 Single



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	4.70	5.30	0.185	0.209
A1	2.20	2.60	0.087	0.102
A2	1.50	2.49	0.059	0.098
b	1.04	1.33	0.041	0.052
b2	1.90	2.41	0.075	0.095
b4	2.87	3.43	0.113	0.135
c	0.55	0.70	0.022	0.028
D	20.70	21.30	0.815	0.839
D1	16.25	17.65	0.640	0.695
D2	0.51	1.40	0.020	0.055
e	5.44 BSC.		0.214 BSC.	
E	15.50	16.30	0.610	0.642
E1	13.08	14.16	0.515	0.557
E2	3.80	5.49	0.150	0.216
E3	1.00	2.75	0.039	0.108
L	19.72	20.32	0.776	0.800
L1	3.85	4.50	0.152	0.177
Q	5.25	6.25	0.207	0.246
P	3.50	3.70	0.138	0.146
S	6.04	6.30	0.238	0.248