

## General Description

The MY5N30D is silicon N-CH Enhanced VDMOSFETS is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency.

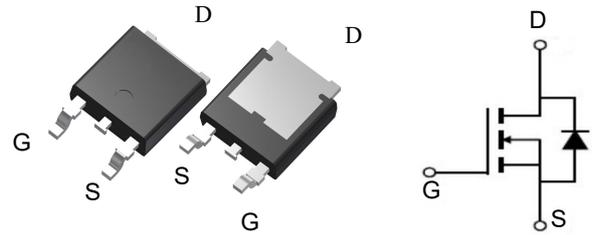


## Features

$V_{DSS}$	300	V
$I_D$	5	A
$P_D(T_C=25^\circ\text{C})$	58.7	W
$R_{DS(ON)}(at V_{GS}=4.5V)$	<1.5	$\Omega$

## Application

- Uninterruptible Power Supply(UPS)
- Power Factor Correction (PFC)



## Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY5N30D	TO-252-2L	MY5N30D	2500

## Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage ( $V_{GS} = 0V$ )	$V_{DSS}$	300	V
Continuous Drain Current	$I_D$	5	A
Pulsed Drain Current	$I_{DM}$	20	A
Gate-Source Voltage	$V_{GSS}$	$\pm 25$	V
Single Pulse Avalanche Energy	$E_{AS}$	50	mJ
Avalanche Current	$I_{AR}$	3.2	A
Repetitive Avalanche Energy	$E_{AR}$	1.5	mJ
Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_D$	58.7	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55~+150	$^\circ\text{C}$
Thermal Resistance, Junction-to - Case	$R_{thJC}$	2.13	$^\circ\text{C/W}$
Thermal Resistance, Junction-to - Ambient	$R_{thJA}$	60	

**Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

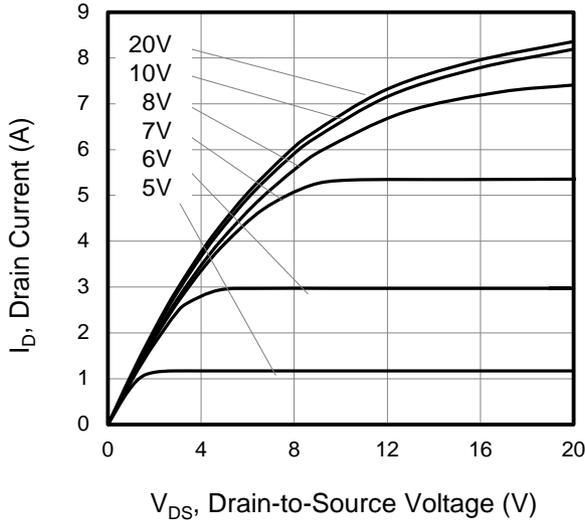
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	300	--	--	V
Zero Gate Voltage Drain Current	IDSS	V <sub>DS</sub> = 300V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 25°C	--	--	1	μA
		V <sub>DS</sub> = 240V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C	--	--	100	
Gate-Source Leakage	IGSS	V <sub>GS</sub> = ±25V	--	--	±100	nA
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	2.2	--	3.2	V
Drain-Source On-Resistance (Note3)	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10V, I <sub>D</sub> = 2.5A	--	1.2	1.5	Ω
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1.0MHz	--	291	--	pF
Output Capacitance	C <sub>oss</sub>		--	43	--	
Reverse Transfer Capacitance	C <sub>rss</sub>		--	7	--	
Total Gate Charge	Q <sub>g</sub>	V <sub>DD</sub> = 240V, I <sub>D</sub> = 5.0A, V <sub>GS</sub> = 10V	--	8.4	--	nC
Gate-Source Charge	Q <sub>gs</sub>		--	1.2	--	
Gate-Drain Charge	Q <sub>gd</sub>		--	3.3	--	
Turn-on Delay Time	td(on)	V <sub>DD</sub> = 150V, I <sub>D</sub> = 5.0A, R <sub>G</sub> = 25 Ω	--	20	--	ns
Turn-on Rise Time	t <sub>r</sub>		--	50	--	
Turn-off Delay Time	td(off)		--	70	--	
Turn-off Fall Time	t <sub>f</sub>		--	53	--	
Continuous Body Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	--	--	5	A
Pulsed Diode Forward Current	I <sub>SM</sub>		--	--	20	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25°C, I <sub>SD</sub> = 5A, V <sub>GS</sub> = 0V	--	--	1.4	V
Reverse Recovery Time	t <sub>rr</sub>	V <sub>GS</sub> = 0V, I <sub>S</sub> = 5A, di <sub>F</sub> /dt = 100A /μs	--	263	--	ns
Reverse Recovery Charge	Q <sub>rr</sub>		--	1.9	--	μC

**Notes**

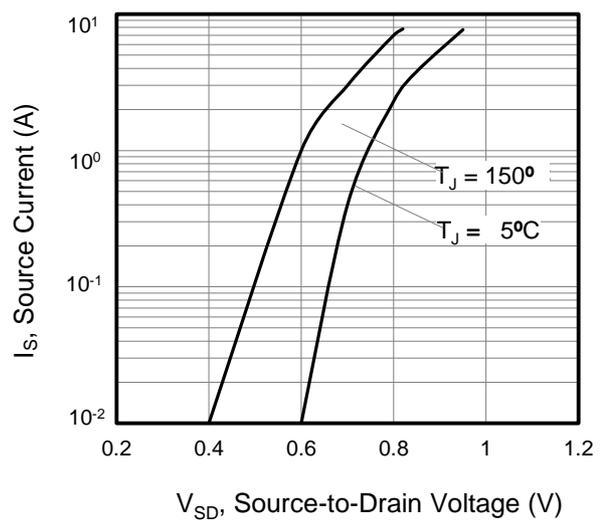
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. I<sub>AS</sub> = 3.2A, V<sub>DD</sub> = 50V, R<sub>G</sub> = 25 Ω, Starting T<sub>J</sub> = 25 °C
3. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 1%

**Typical Characteristics**

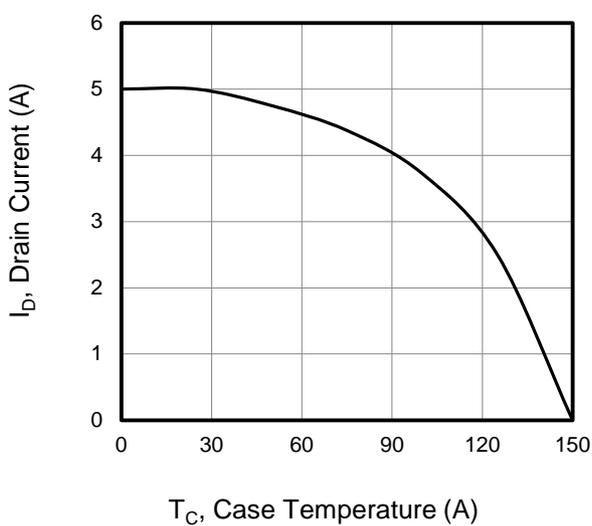
**Figure 1. Output Characteristics ( $T_J = 25^\circ\text{C}$ )**



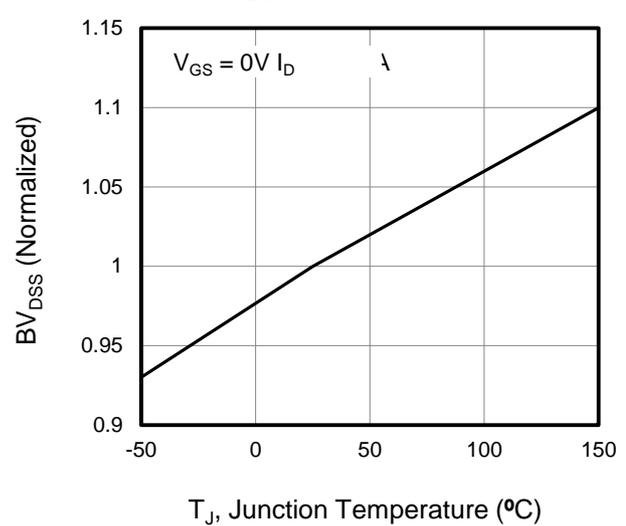
**Figure 2. Body Diode Forward Voltage**



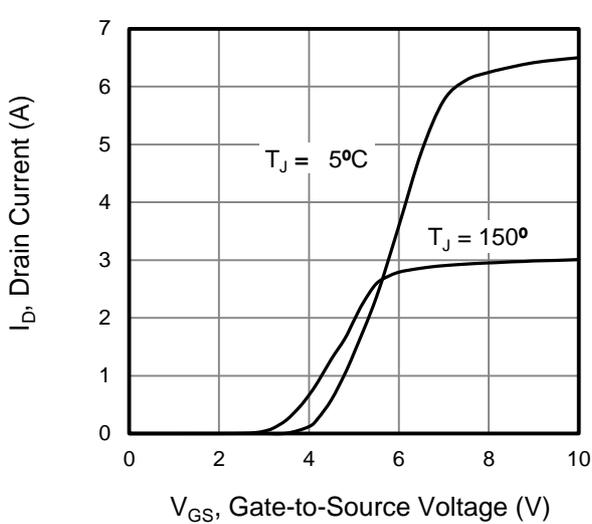
**Figure 3. Drain Current vs. Temperature**



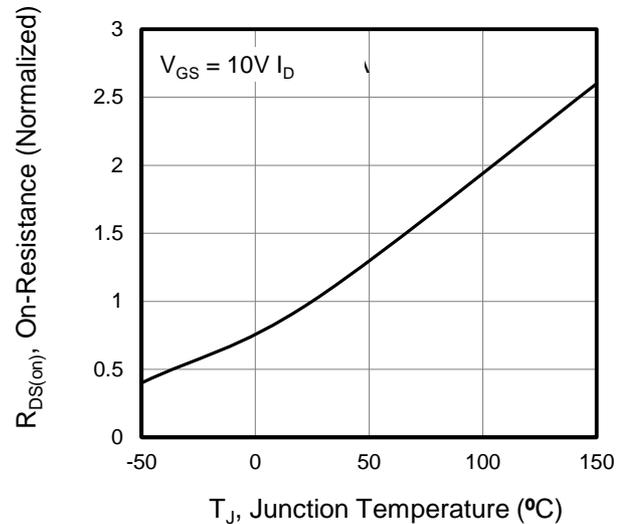
**Figure 4.  $BV_{DSS}$  Variation vs. Temperature**



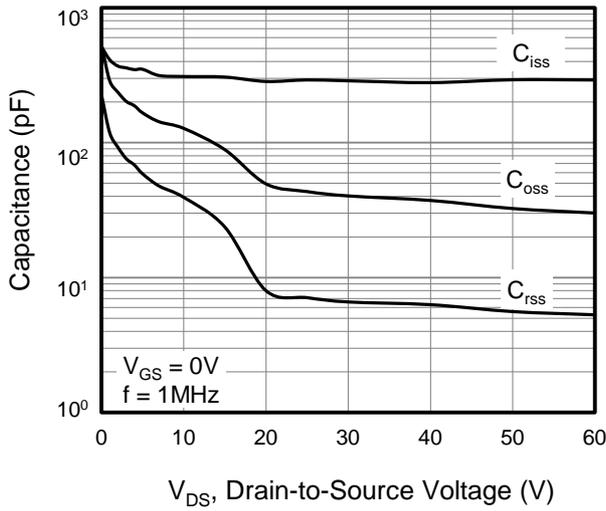
**Figure 5. Transfer Characteristics**



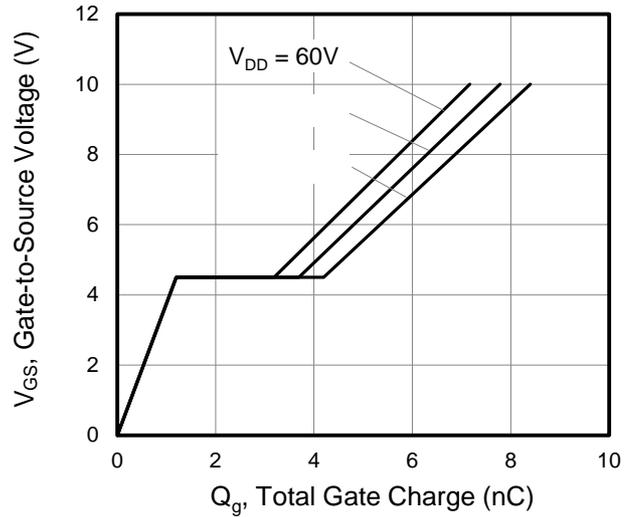
**Figure 6. On-Resistance vs. Temperature**



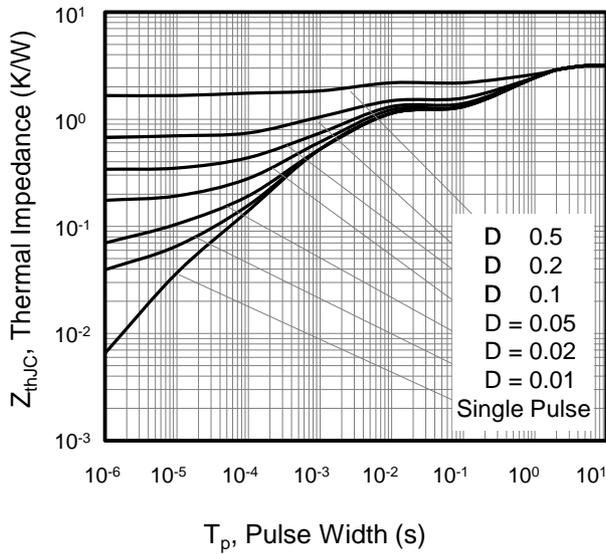
**Figure 7. Capacitance**



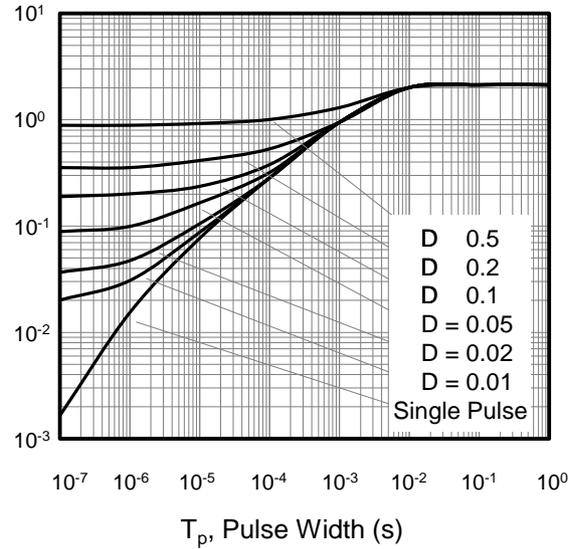
**Figure 8. Gate Charge**



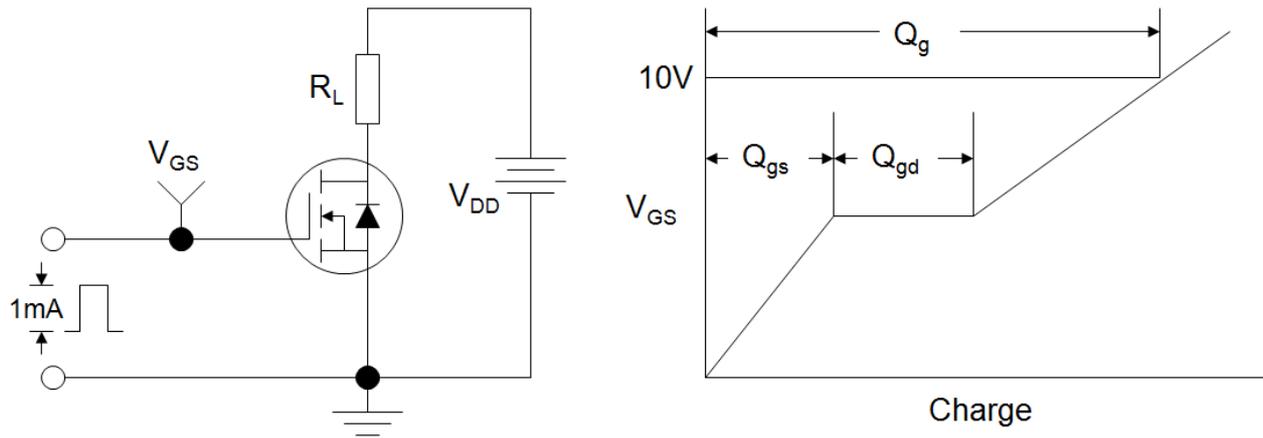
**Figure 9. Transient Thermal Impedance TO-220F**



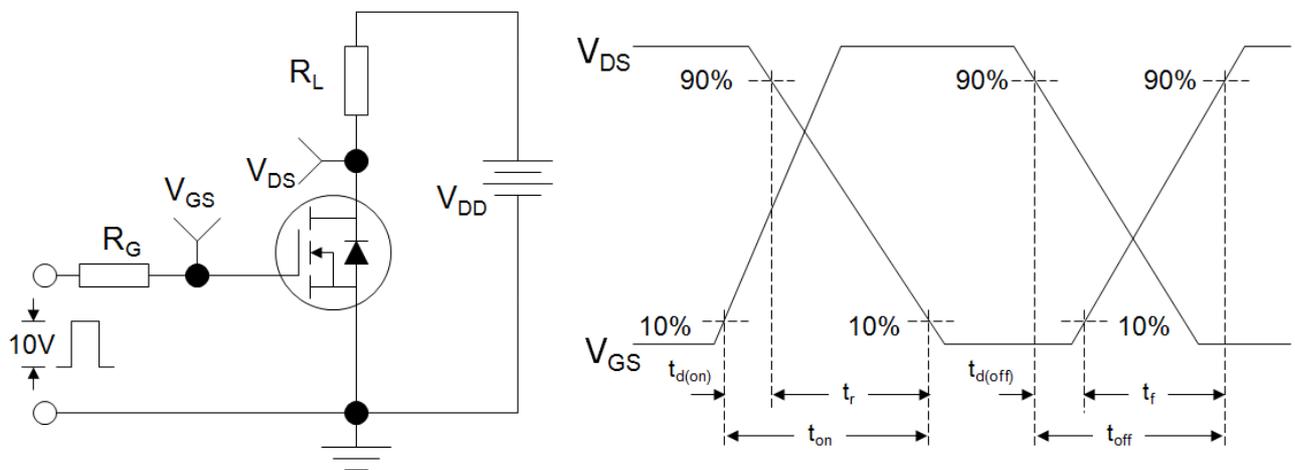
**Figure 10. Transient Thermal Impedance TO-251, TO-252**



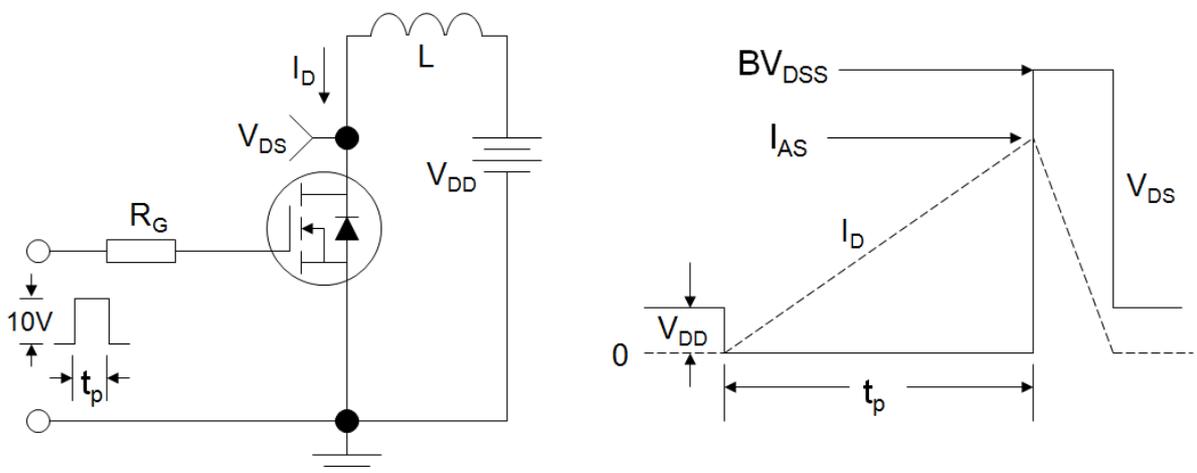
**Figure A: Gate Charge Test Circuit and Waveform**



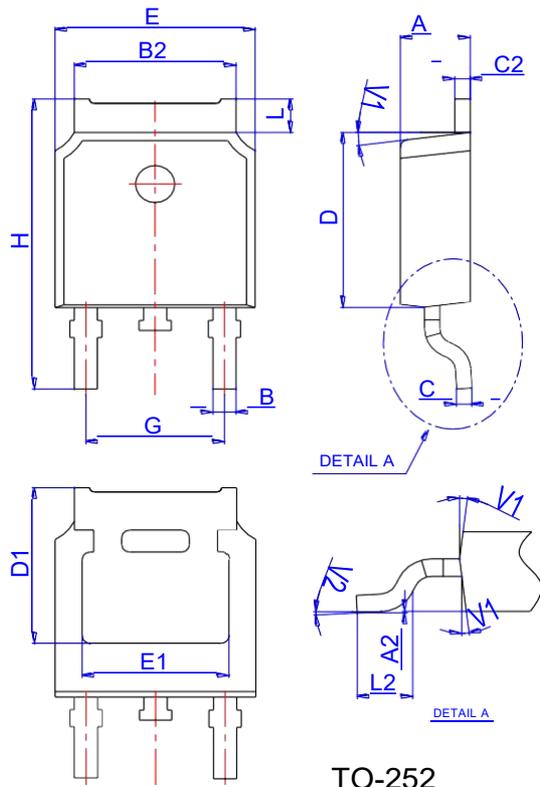
**Figure B: Resistive Switching Test Circuit and Waveform**



**Figure C: Unclamped Inductive Switching Test Circuit and Waveform**

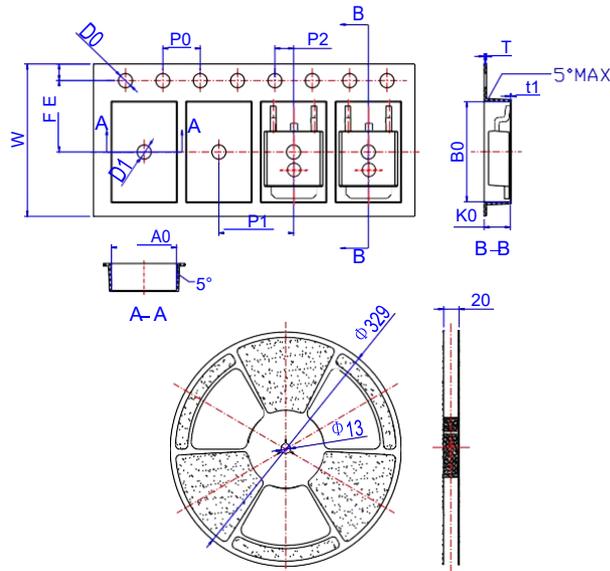


**Package Mechanical Data-TO-252-JQ Single**



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

**Reel Specification-TO-252**



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583