General Description

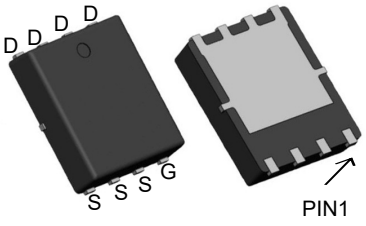
The MY50P03NE5 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

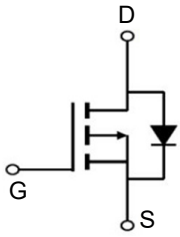
Features

V_{DSS}	-30	V
I_D	-50	A
$R_{DS(ON)}$(atV_{GS} =10V)	11.5	mÝ
$R_{DS(ON)}$(atV_{GS} =4.5V)	18	mÝ

Application

- Battery protection
- Load switch
- Uninterruptible power supply





Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY50P03NE5	PDFN5*6-8L	NULL	5000

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	VDS	-30	V
Gate-Source Voltage	VGS	±20	V
Drain Current-Continuous (T_C=25℃)	I_D	-50	A
Drain Current-Continuous (T_C=100℃)		-24	
Drain Current-Pulsed (Note 1)	IDM	-80	A
Maximum Power Dissipation (T_C=25℃)	P_D	3	W
Maximum Power Dissipation (T_C=100℃)		1.3	
Single pulse avalanche energy (Note 5)	EAS	231	mJ
Operating Junction and Storage Temperature Range	TJ,TSTG	-55 To 150	℃
Thermal Resistance,Junction-to-Ambient (Note 2)	RθJA	41.67	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-30	-33	-	V
Zero Gate Voltage Drain Current	IDSS	V_{DS}=-30V,V_{GS}=0V	-	-	-1	μA
Gate-Body Leakage Current	IGSS	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	VGS(th)	V_{DS}=V_{GS},I_D=-250μA	-1	-1.5	-3	V
Drain-Source On-State Resistance	RDS(ON)	V_{GS}=-10V, I_D=-10A	-	11.5	15	mΩ
		V_{GS}=-4.5V, I_D=-7A	-	18	25	mΩ
Forward Transconductance	gFS	V_{DS}=-10V,I_D=-10A	-	20	-	S
Input Capacitance	C_{lss}	V_{DS}=-15V,V_{GS}=0V, F=1.0MHz	-	1750	-	PF
Output Capacitance	Coss		-	215	-	PF
Reverse Transfer Capacitance	C_{rss}		-	180	-	PF
Turn-on Delay Time	td(on)	V_{DD}=-15V, ID=-10A, V_{GS}=-10V,R_{GEN}=1Ω	-	9	-	nS
Turn-on Rise Time	t_r		-	8	-	nS
Turn-Off Delay Time	td(off)		-	28	-	nS
Turn-Off Fall Time	t_f		-	10	-	nS
Total Gate Charge	Q_g	V_{DS}=-15V,I_D=-10A,V_{GS}=-10V	-	24	-	nC
Gate-Source Charge	Q_{gs}		-	3.5	-	nC
Gate-Drain Charge	Q_{gd}		-	6	-	nC
Diode Forward Current (Note 2)	I_S		-	-	-12	A
Diode Forward Voltage (Note 3)	VSD	V_{GS}=0V,I_S=-12A	-	-	-1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E_{AS} condition: Tj=25℃,V_{DD}=-15V,V_G=10V,L=0.5mH,Rg=25Ω, I_{AS}=-34A

Typical Characteristics

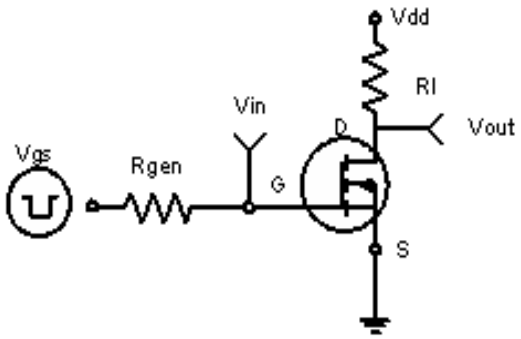


Figure 1:Switching Test Circuit

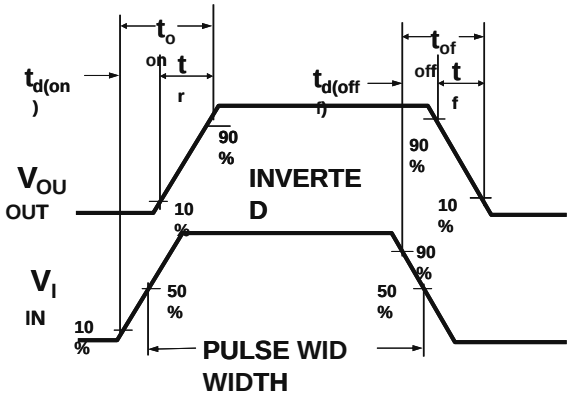


Figure 2:Switching Waveforms

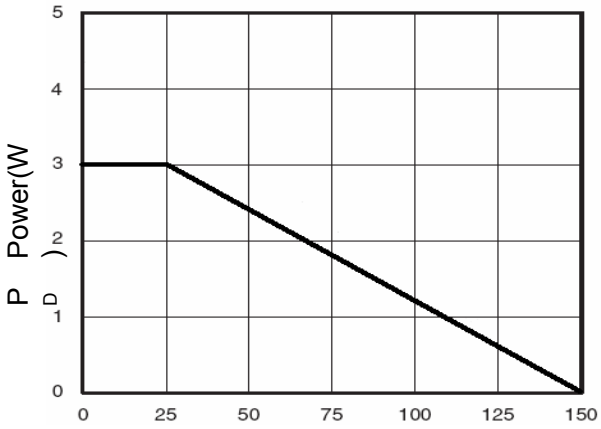


Figure 3 Power Dissipation

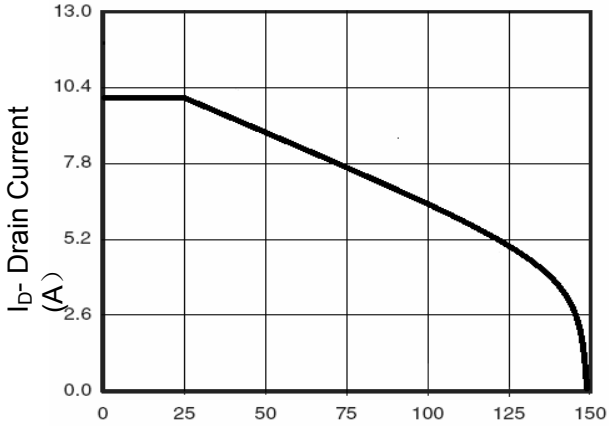


Figure 4 Drain Current

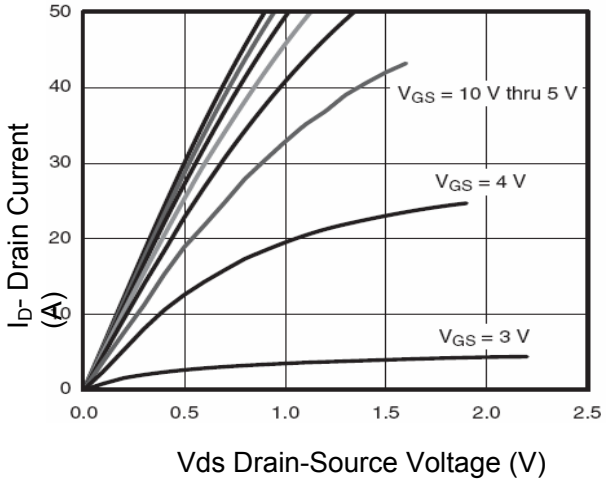


Figure 5 Output Characteristics

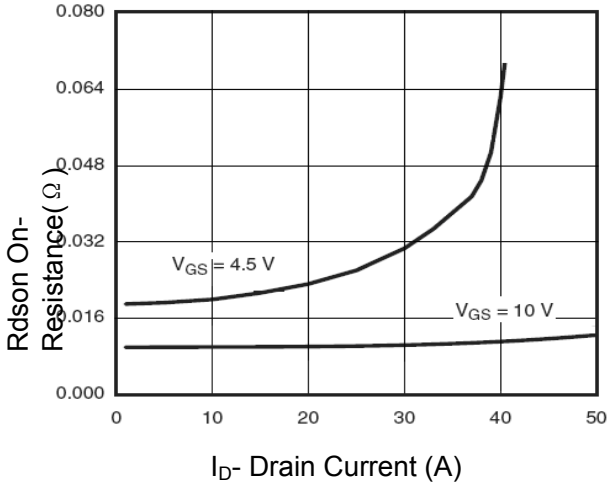
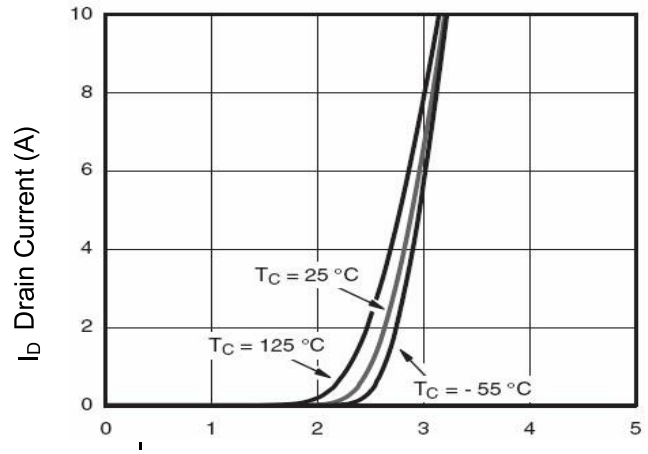
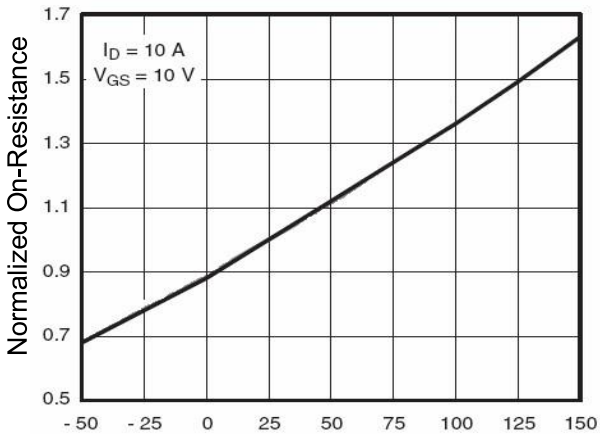


Figure 6 Drain-Source On-Resistance



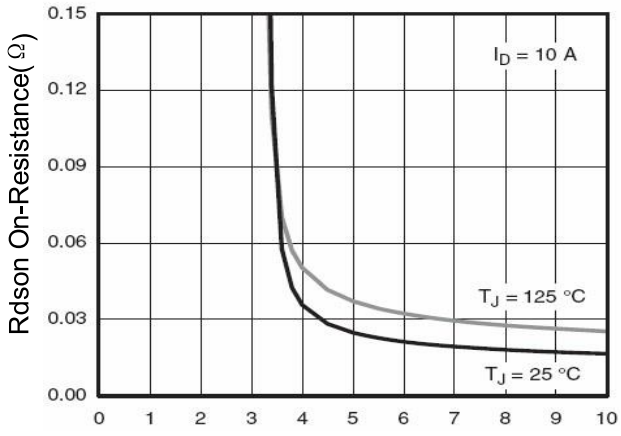
Vgs Gate-Source Voltage (V)

Figure 7 Transfer Characteristics



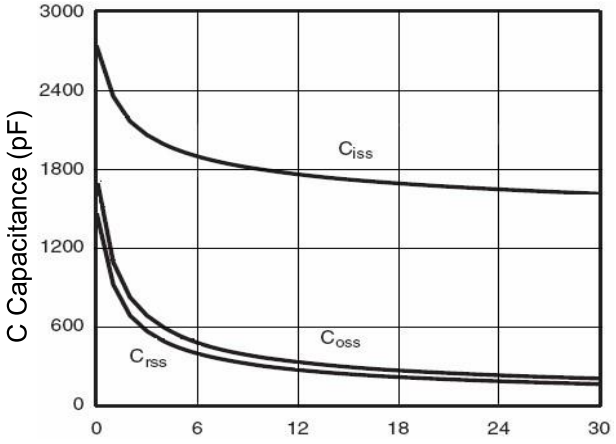
T_J - Junction Temperature (℃)

Figure 8 Drain-Source On-Resistance



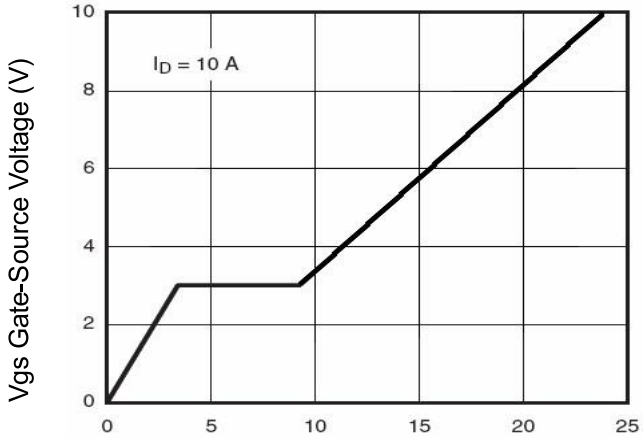
Vgs Gate-Source Voltage (V)

Figure 9 Rdson vs Vgs



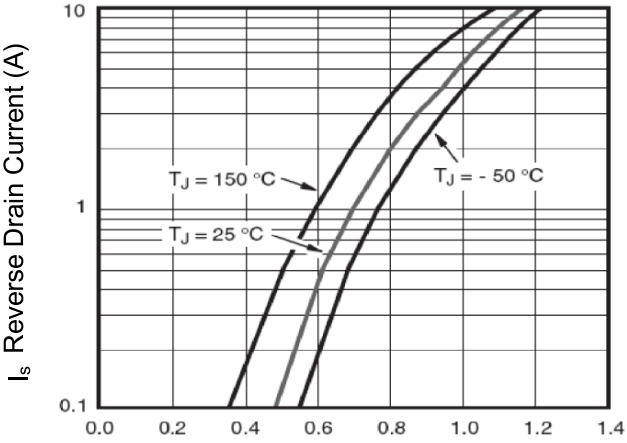
Vds Drain-Source Voltage (V)

Figure 10 Capacitance vs Vds



Qg Gate Charge (nC)

Figure 11 Gate Charge



Vsd Source-Drain Voltage (V)

Figure 12 Source- Drain Diode Forward

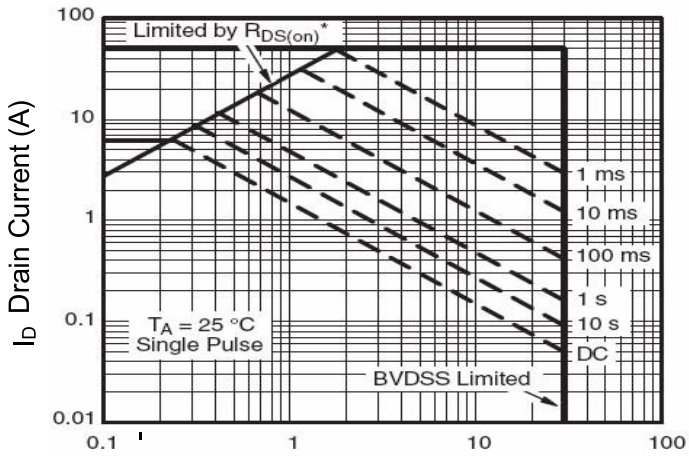


Figure 13 Safe Operation Area

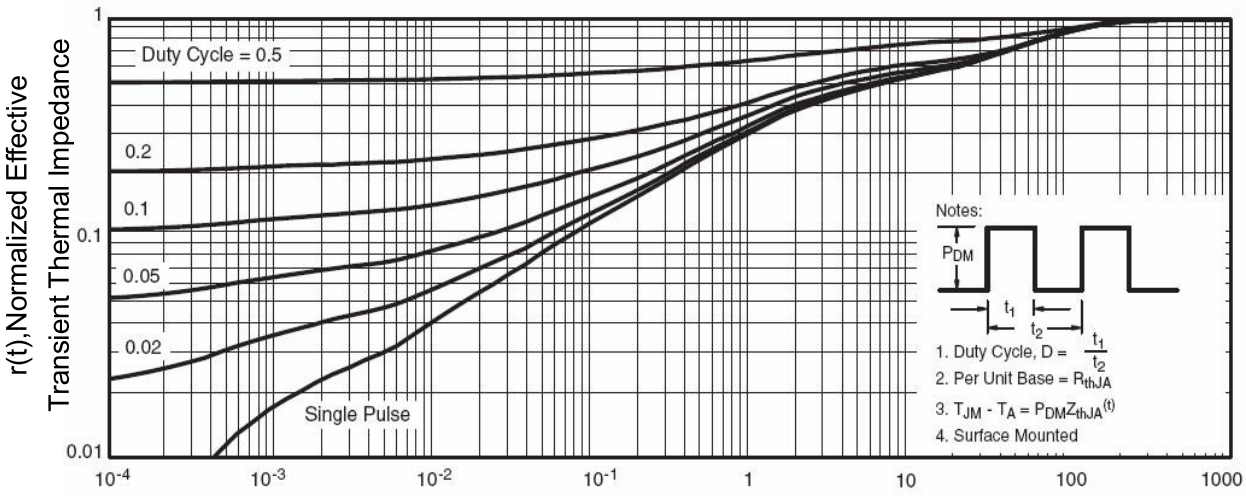
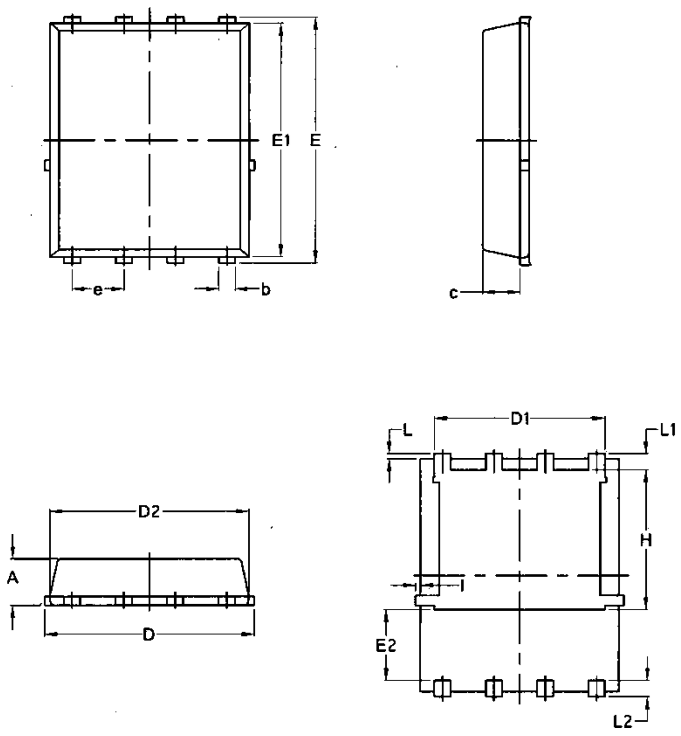


Figure 14 Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-DFN5*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070