

General Description

The MY4409 is the high cell density trenched P-ch MOSFETs, which provide excellent RDS(ON) and gate charge for most of the synchronous buck converter applications.

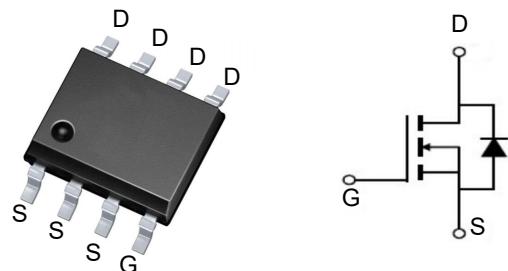


Features

V _{DSS}	30	V
I _D	15	A
R _{DS(ON)} (at V _{GS} =10V)	8	mΩ
R _{DS(ON)} (at V _{GS} =4.5V)	11	mΩ

Application

- Battery protection
- Load switch
- PWM application



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY4409	SOP-8	4409	3000

Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	-30	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ -10V ¹	- 15	A
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ -10V ¹	-9	A
I _{DM}	Pulsed Drain Current ²	-46	A
EAS	Single Pulse Avalanche Energy ³	55	mJ
I _{AS}	Avalanche Current	-50	A
P _D @T _A =25°C	Total Power Dissipation ⁴	4.5	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	75	°C/W
	Thermal Resistance Junction-Ambient ¹ (t≤10s)	---	40	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	24	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(\text{BR})\text{DSS}}$	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}$, $I_D=-250\mu\text{A}$	-30	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-30\text{V}$, $V_{GS}=0\text{V}$,	-	-	-1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=-250\mu\text{A}$	-1.0	-1.6	-2.5	V
$R_{\text{DS(on)}}$ Note3	Static Drain-Source on-Resistance	$V_{GS}=-10\text{V}$, $I_D=-10\text{A}$	-	8	10	$\text{m}\Omega$
		$V_{GS}=-4.5\text{V}$, $I_D=-5\text{A}$	-	11	15	
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=-15\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	1970	-	pF
C_{oss}	Output Capacitance		-	233	-	pF
C_{rss}	Reverse Transfer Capacitance		-	206	-	pF
Q_g	Total Gate Charge	$V_{DS}=-15\text{V}$, $I_D=-5\text{A}$, $V_{GS}=-10\text{V}$	-	22	-	nC
Q_{gs}	Gate-Source Charge		-	1.0	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	1.8	-	nC
Switching Characteristics						
$t_{d(\text{on})}$	Turn-on Delay Time	$V_{DD}=-15\text{V}$, $I_D=-10\text{A}$, $V_{GS}=-10\text{V}$, $R_{\text{GEN}}=2.5\Omega$	-	9	-	ns
t_r	Turn-on Rise Time		-	13	-	ns
$t_{d(\text{off})}$	Turn-off Delay Time		-	48	-	ns
t_f	Turn-off Fall Time		-	20	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_s	Maximum Continuous Drain to Source Diode Forward	-	-	-12	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	-60	A	
V_{SD}	Drain to Source Diode Forward	$V_{GS}=0\text{V}$, $I_s=-15\text{A}$	-	-0.8	-1.2	V
trr	Reverse Recovery Time	$T_J=25^\circ\text{C}$, $V_{DD}=-24\text{V}$, $I_F=-2.8\text{A}$, $dI/dt=-100\text{A}/\mu\text{s}$	-	64	-	ns
Q_{rr}	Reverse Recovery Charge		-	25	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: $T_J=25^\circ\text{C}$, $V_{GS}=10\text{V}$, $R_G=25\Omega$, $L=0.5\text{mH}$, $I_{AS}=-12.7\text{A}$

3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$

Typical Characteristics

Figure 1: Output Characteristics

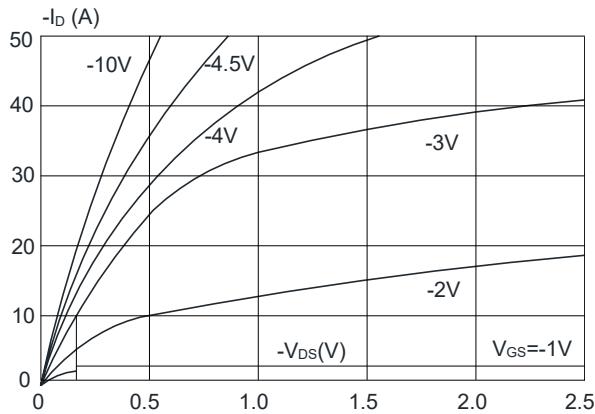


Figure 3: On-resistance vs. Drain Current

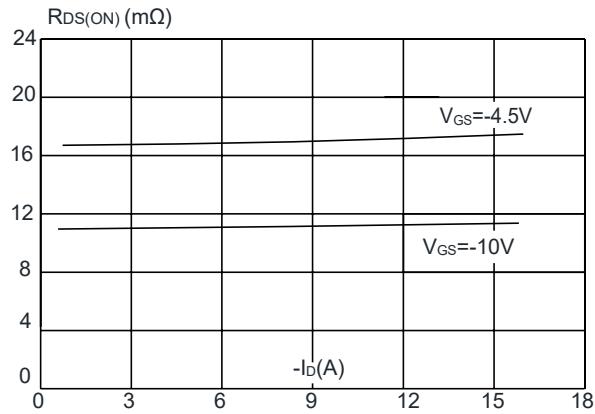


Figure 5: Gate Charge Characteristics

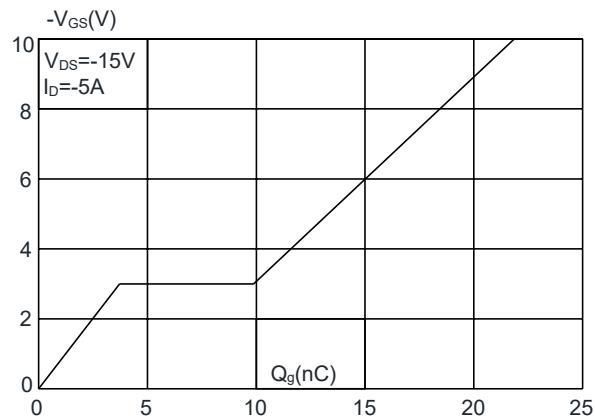


Figure 2: Typical Transfer Characteristics

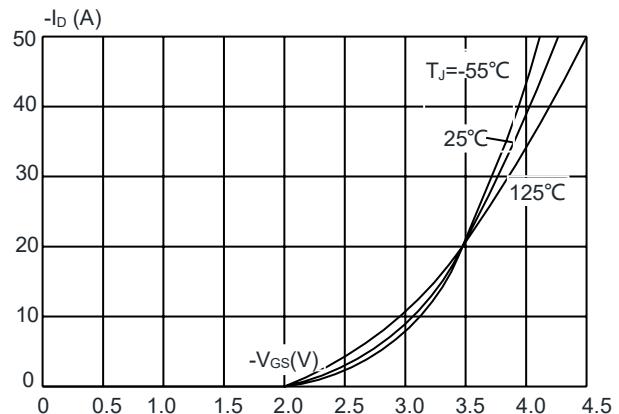


Figure 4: Body Diode Characteristics

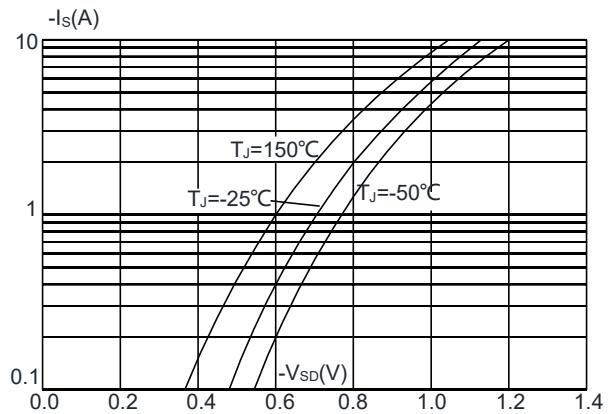


Figure 6: Capacitance Characteristics

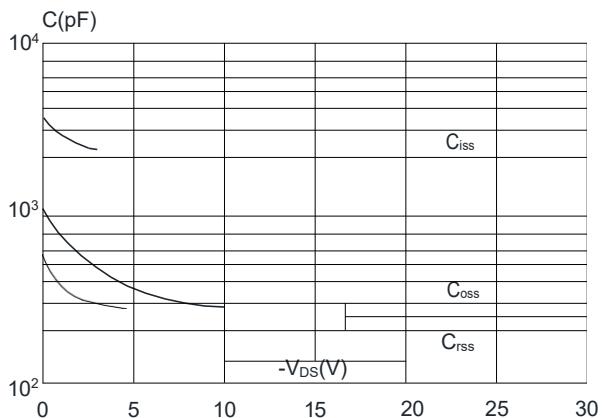


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

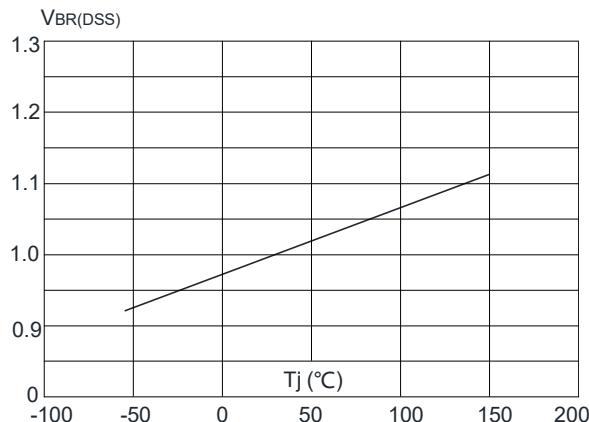


Figure 8: Normalized on Resistance vs. Junction Temperature

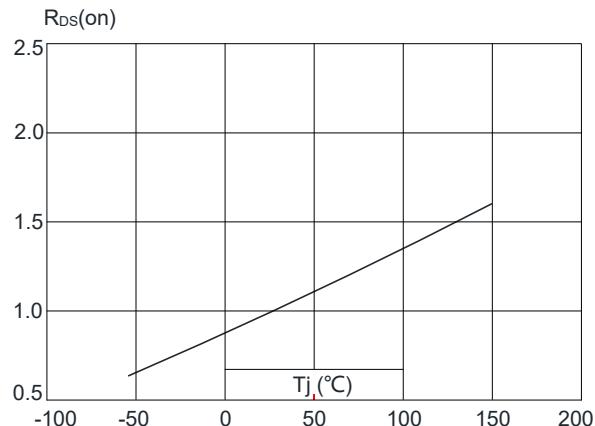


Figure 9: Maximum Safe Operating Area

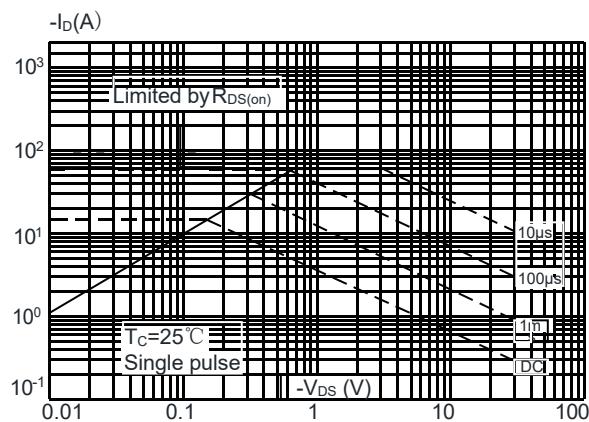


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

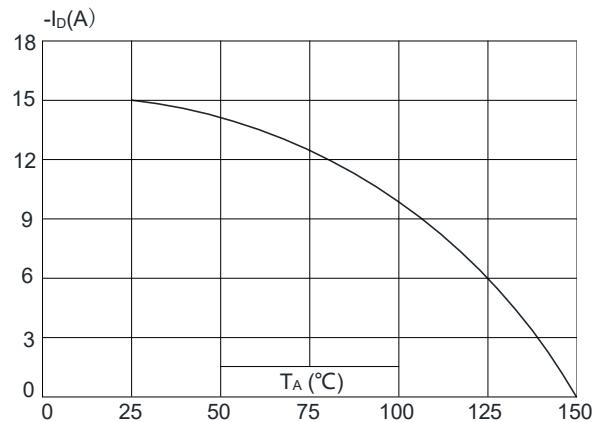
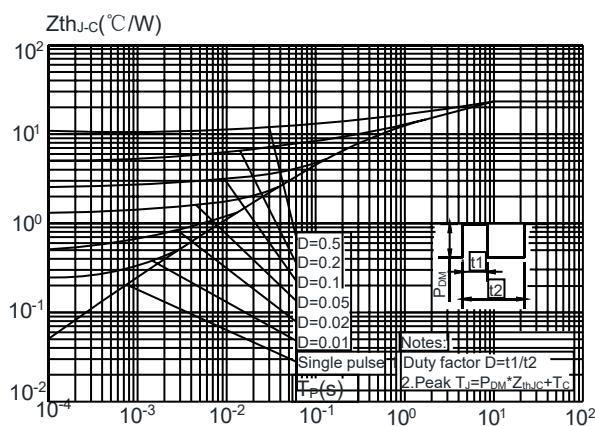
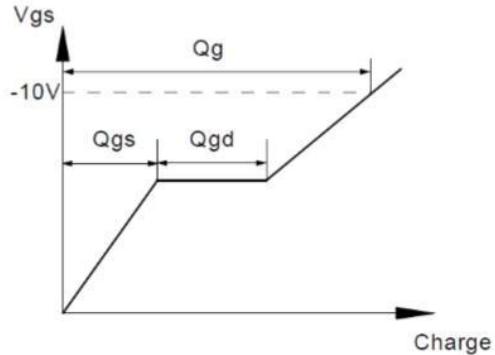
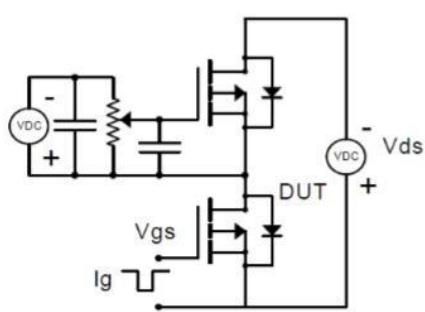


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

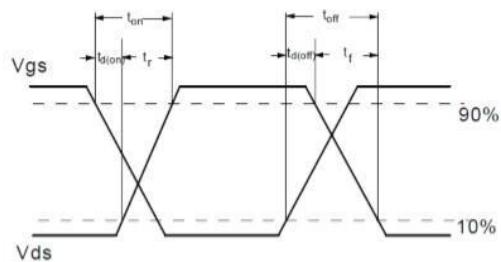
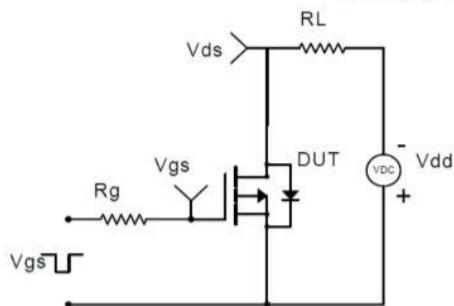


Test Circuit

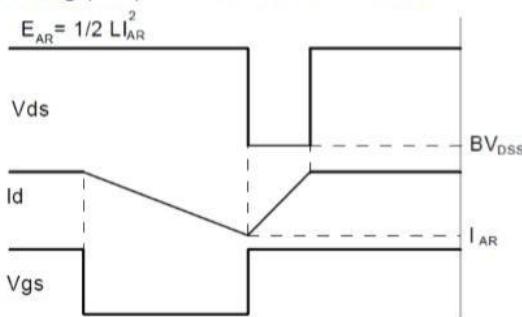
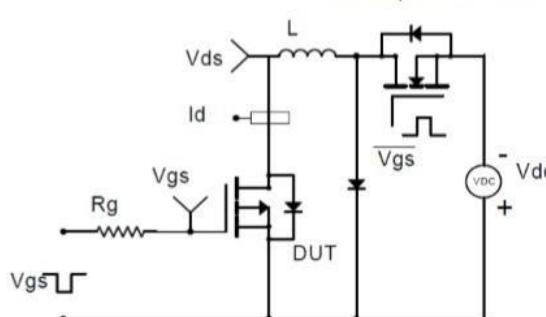
Gate Charge Test Circuit & Waveform



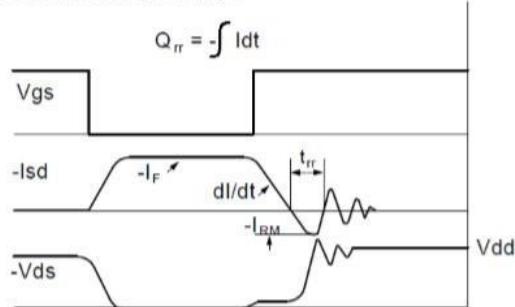
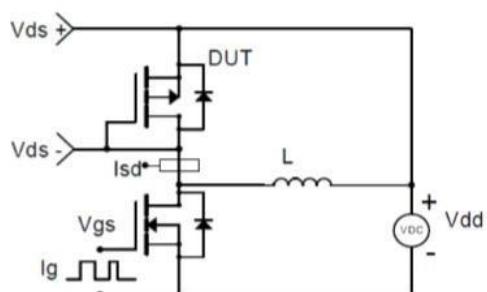
Resistive Switching Test Circuit & Waveforms



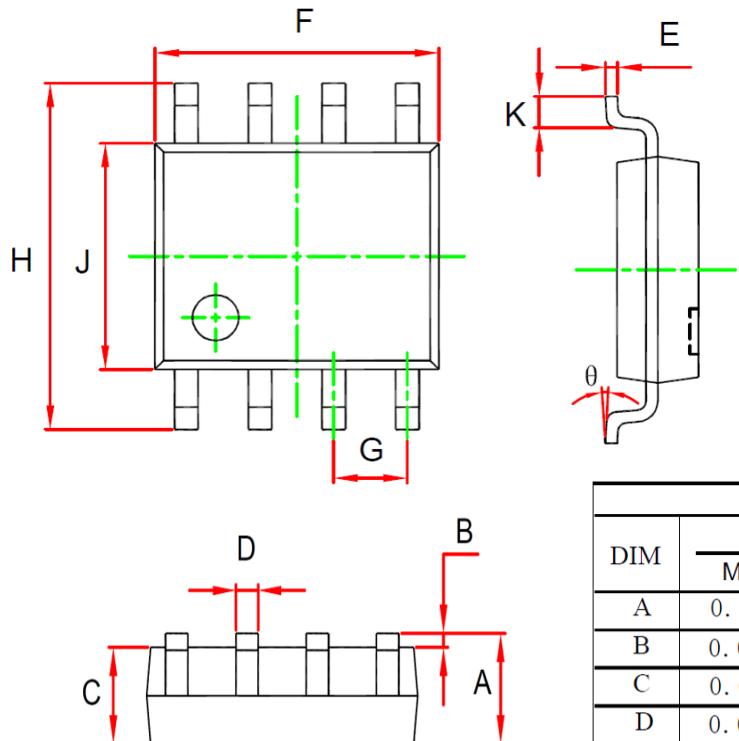
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Mechanical Data-SOP-8



DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.350	1.750	
B	0.004	0.010	0.100	0.250	
C	0.053	0.061	1.350	1.550	
D	0.013	0.020	0.330	0.510	
E	0.007	0.010	0.170	0.250	
F	0.189	0.197	4.800	5.000	
G	0.050 (BSC)		1.270	(BSC)	
H	0.228	0.244	5.800	6.200	
J	0.150	0.157	3.800	4.000	
K	0.016	0.050	0.400	1.270	
θ	0°	8°	0°	8°	