

General Description

The MY16N50F is silicon N-channel Enhanced VDMOSFETS, obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy.

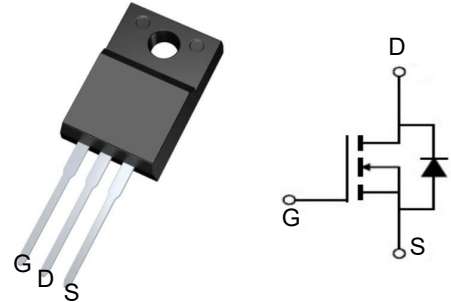


Features

V_{DSS}	500	V
I_D	15	A
P_D ($T_C = 25\text{ }^{\circ}\text{C}$)	52	W
$R_{DS(ON)}$ (at $V_{GS} = 10\text{V}$)	0.5	Ω

Application

- High efficiency switch mode power supplies
- Power factor correction
- Electronic lamp ballast



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY16N50F	TO-220F	MY16N50F	1000

Absolute Maximum Ratings ($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameters	Ratings	Unit
V_{DSS}	Drain-Source Voltage	500	V
V_{GS}	Gate-Source Voltage-Continuous	± 30	V
I_D	Drain Current-Continuous (Note 2)	15	A
I_{DM}	Drain Current-Single Plused (Note 1)	60	A
P_D	Power Dissipation (Note 2)	52	W
T_j	Max.Operating junction temperature	150	$^{\circ}\text{C/W}$

Electrical Characteristics ($T_c=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameters	Min	Typ	Max	Units	Conditions
Static Characteristics						
B _{VDSS}	Drain-Source Breakdown VoltageCurrent (Note 1)	500	--	--	mA	I _D =250μA V _{GS} =0V , T _J =25°C
V _{GS(th)}	Gate Threshold Voltage	2.0	--	4.0	V	V _{DS} =V _{GS} , I _D =250μA
R _{DS(on)}	Drain-Source On-Resistance	--	0.5	0.75	Ω	V _{GS} =10V , I _D =7.5A
I _{GSS}	Gate-Body Leakage Current	--	--	±100	nA	V _{GS} =±30V , V _{DS} =0
I _{DSS}	Zero Gate Voltage Drain Current	--	--	1	μA	V _{DS} =500V , V _{GS} =0
g _{fs}	Forward Transconductance	--	4.0	--	S	V _{DS} =40V, I _D =7.5A
Switching Characteristics						
T _{d (on)}	Turn-On Delay Time	--	55	120	ns	V _{DS} =250V , I _D =15A, R _G =25Ω (Note 2)
T _r	Rise Time	--	160	340	ns	
T _{d (off)}	Turn-Off Delay Time	--	130	280	ns	
T _f	Fall Time	--	100	195	ns	
Q _g	Total Gate Charge	--	45	62	nC	V _{DS} =400V, V _{GS} =10V I _D =15A (Note 2)
Q _{gs}	Gate-Source Charge	--	8.5	--	nC	
Q _{gd}	Gate-Drain Charge	--	18.5	--	nC	
Dynamic Characteristics						
C _{iss}	Input Capacitance	--	1580	2655	pF	V _{DS} =25V , V _{GS} =0, f=1MHz
C _{oss}	Output Capacitance	--	230	315	pF	
C _{rss}	Reverse Transfer Capacitance	--	25	40	pF	
I _S	Continuous Drain-Source Diode ForwardCurrent (Note 2)	--	--	16	A	
V _{SD}	Diode Forward On-Voltage	--	--	1.4	V	I _S =15A , V _{GS} =0
R _{th(j-c)}	Thermal Resistance, Junction to Case	--	--	0.65	°C/W	

Note 1: Repetitive Rating : Pulse width limited by maximum junction temperature

Note 2: Pulse test: $PW \leq 300\mu\text{s}$, duty cycle $\leq 2\%$.

Ratings and Characteristic curves

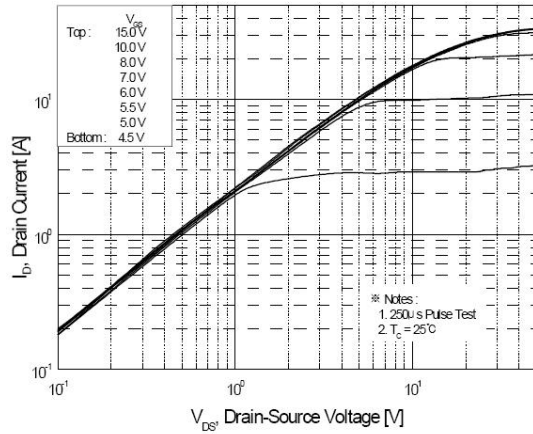


Figure 1. On-Region Characteristics

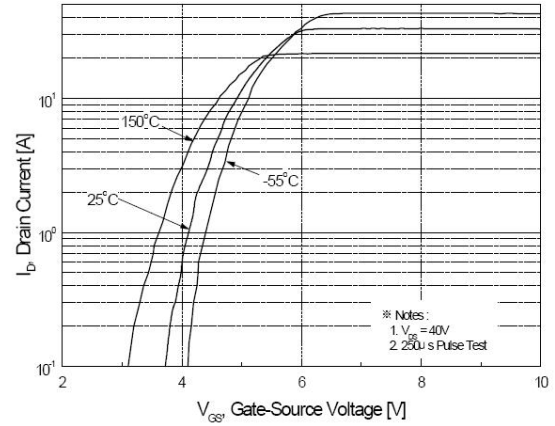


Figure 2. Transfer Characteristics

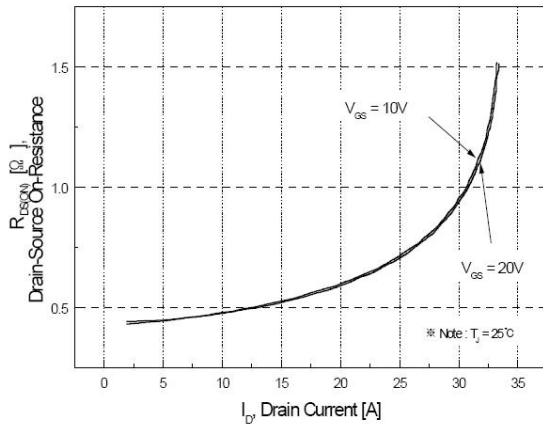


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

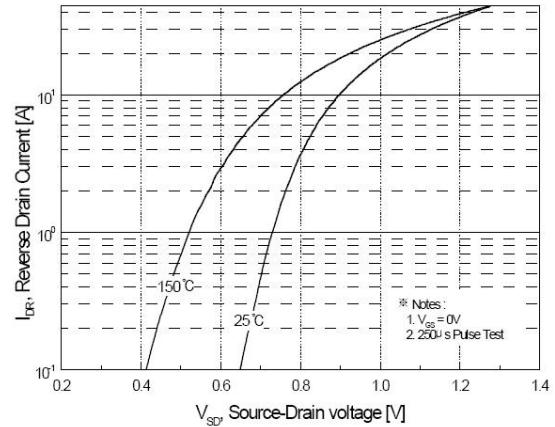


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

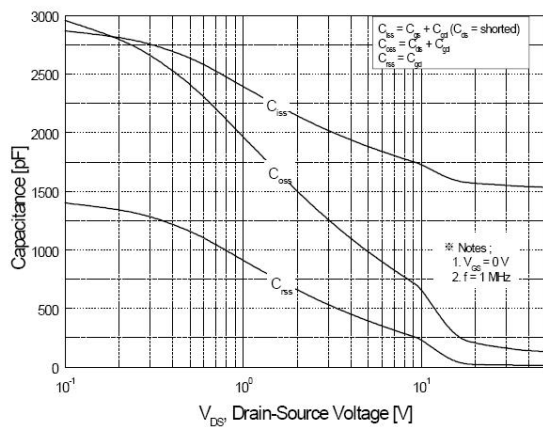


Figure 5. Capacitance Characteristics

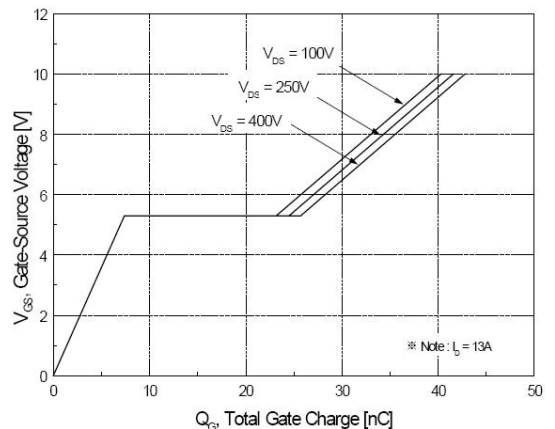


Figure 6. Gate Charge Characteristics

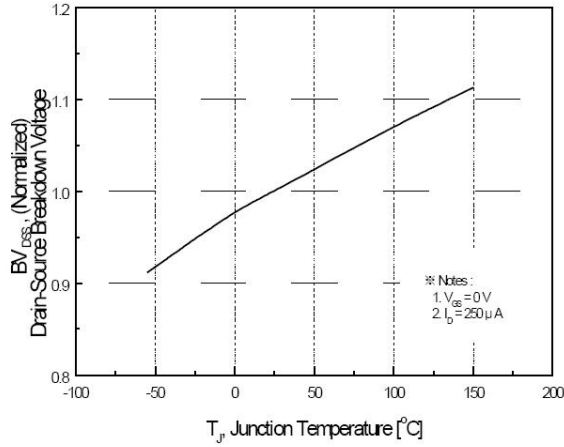


Figure 7. Breakdown Voltage Variation vs Temperature

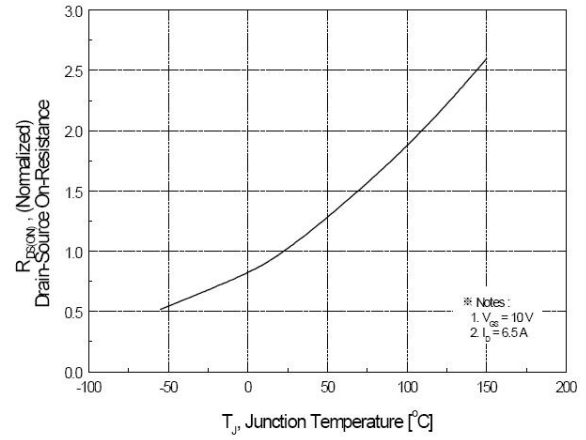


Figure 8. On-Resistance Variation vs Temperature

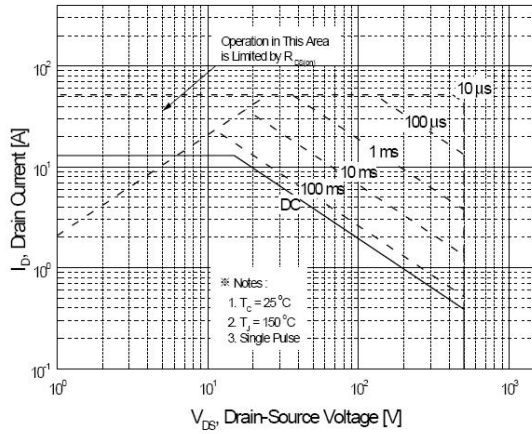


Figure 9. Maximum Safe Operating Area

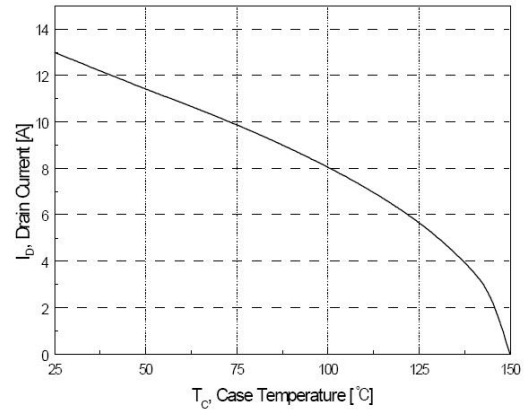


Figure 10. Maximum Drain Current vs Case Temperature

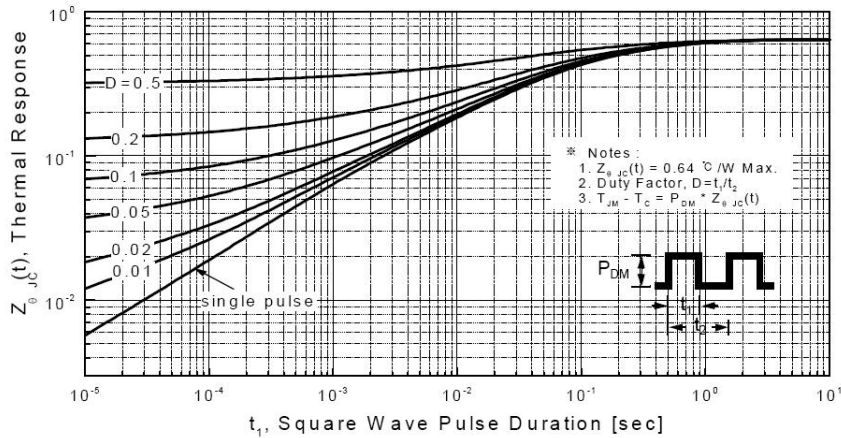


Figure 11. Transient Thermal Response Curve

Fig 12. Gate Charge Test Circuit & Waveform

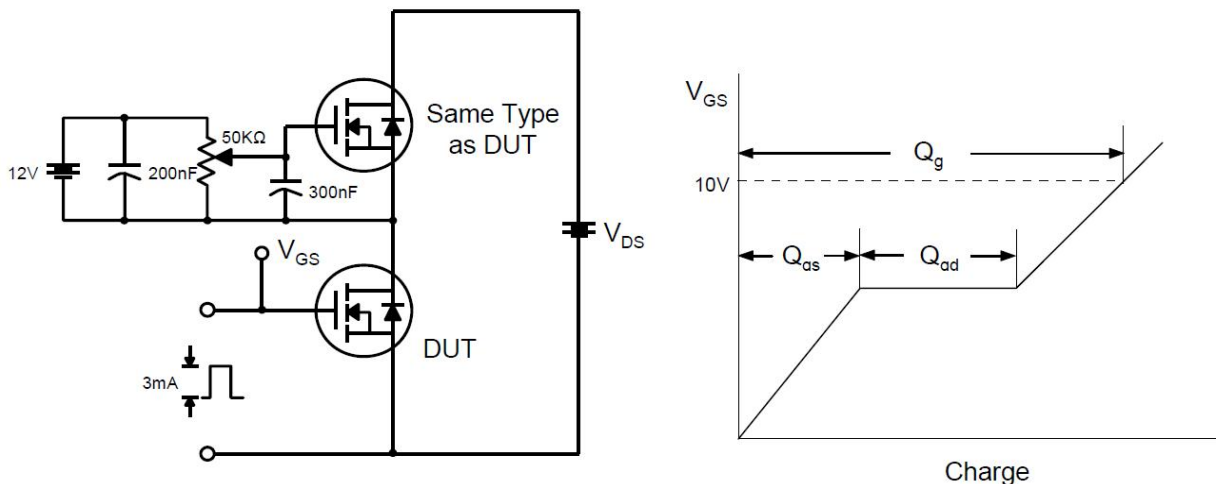


Fig 13. Resistive Switching Test Circuit & Waveforms

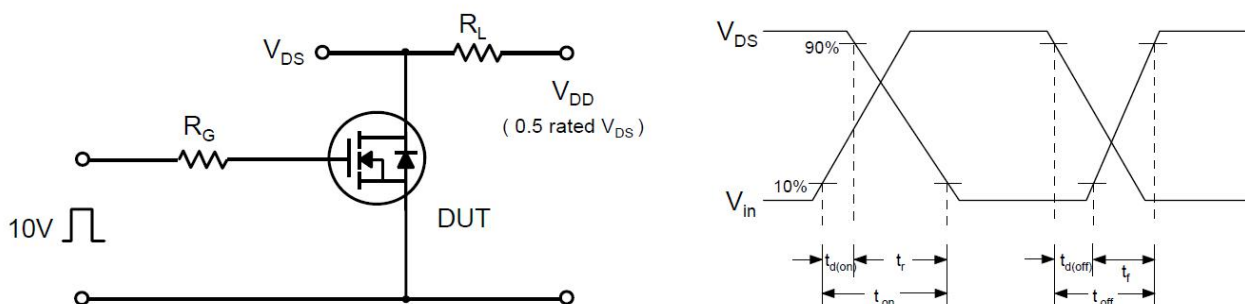


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

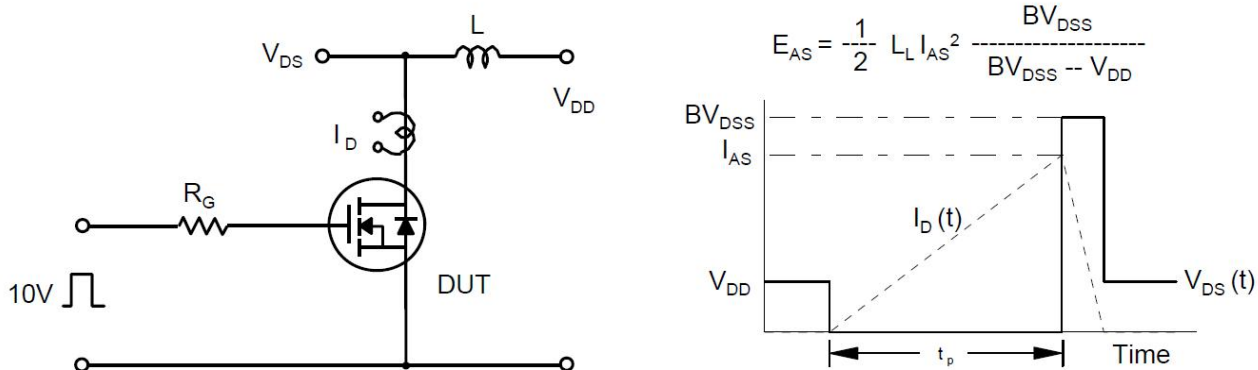
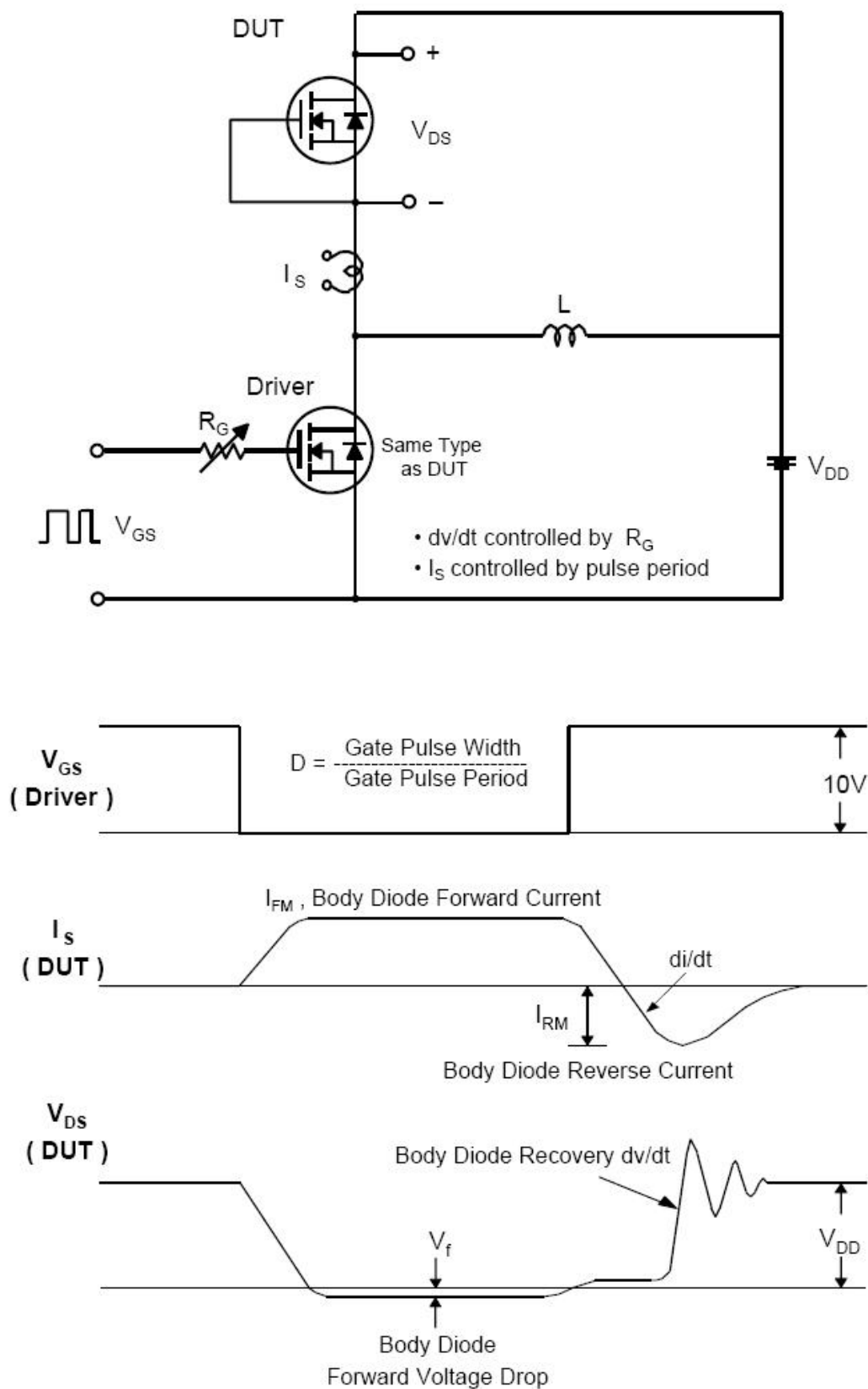
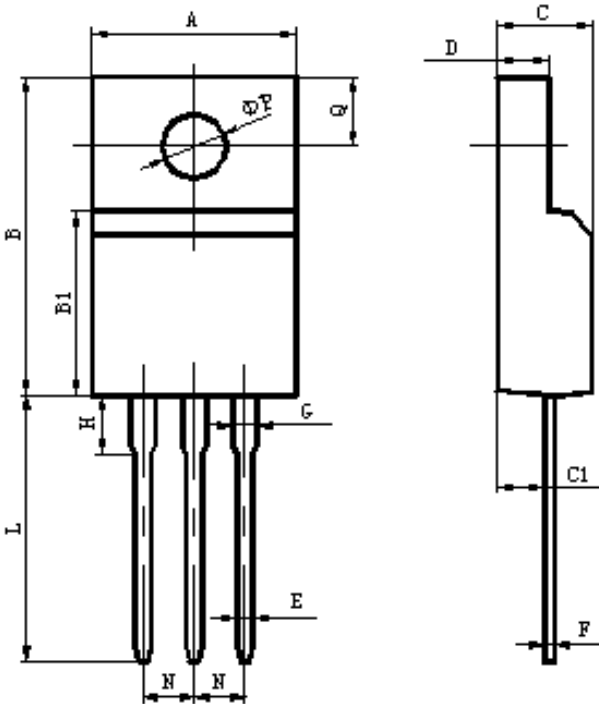


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Mechanical Data-TO-220F Single



Items	Values(mm)	
	MIN	MAX
A	9.60	10.4
B	15.4	16.2
B1	8.90	9.50
C	4.30	4.90
C1	2.10	3.00
D	2.40	3.00
E	0.60	1.00
F	0.30	0.60
G	1.12	1.42
H	3.40	3.80
	2.40	2.90
L*	12.0	14.0
N	2.34	2.74
Q	3.15	3.55
Φ P	2.90	3.30