General Description

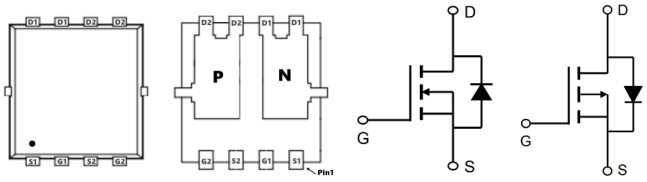
The MY15G02E is the high performance complementary N-ch and P-ch MOSFETs with high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications . The MY15G02E meet the RoHS and Green Product requirement 100% EAS guaranteed with full function eliability appoved.

Features

V_{DSS}	20	-20	V
I_D	60	-40	A
$R_{DS(ON)}$(atV_{GS}=10V)	4.8		mΩ
$R_{DS(ON)}$(atV_{GS}=4.5V)	6.2		mΩ
$R_{DS(ON)}$(atV_{GS}=-10V)	15.5		mΩ
$R_{DS(ON)}$(atV_{GS}=-4.5V)	22		mΩ

Application

- 100% EAS Guaranteed
- Green Device Available
- Super Low Gate Charge
- Excellent CdV/dt effect decline



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY15G02E	PDFN3*3-8L	MY15G02E	5000

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	±12	±12	V
I_D@Ta=25℃	Continuous Drain Current, V_{GS} @ 10V[1]	60	-40	A
I_D@Ta=100℃	Continuous Drain Current, V_{GS} @ 10V[1]	35	-18	A
I_{DM}	Pulsed Drain Current[2]	82	-62	A
EAS	Single Pulse Avalanche Energy[3]	28	66	mJ
P_D@T_C=25℃	Total Power Dissipation[4]	15	21.3	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	℃

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	---	62	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case[1]	---	6	℃/W

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=20V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±12V,V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	0.5	0.75	1.0	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=20 A	-	4.8	6	mΩ
		V_{GS}=2.5V, I_D=15A		6.2	9	mΩ
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=20A	15	-	-	S
Input Capacitance	C_{lss}	V_{DS}=10V,V_{GS}=0V, F=1.0MHz	-	2000	-	PF
Output Capacitance	C_{oss}		-	500	-	PF
Reverse Transfer Capacitance	C_{rss}		-	200	-	PF
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=10V,I_D=2A,R_L=1Ω V_{GS}=4.5V,R_G=3Ω	-	6.4	-	nS
Turn-on Rise Time	t_r		-	17.2	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	29.6	-	nS
Turn-Off Fall Time	t_f		-	16.8	-	nS
Total Gate Charge	Q_g	V_{DS}=10V,I_D=20A, V_{GS}=10V	-	27		nC
Gate-Source Charge	Q_{gs}		-	6.5		nC
Gate-Drain Charge	Q_{gd}		-	6.4		nC
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=10A	-		1.2	V
Diode Forward Current (Note 2)	I_S		-	-	60	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF = 20A di/dt = 100A/μs (Note3)	-	25	-	nS
Reverse Recovery Charge	Qrr		-	24	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Note :

1. The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦2%
3. The EAS data shows Max. rating . The test condition isV_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=20A
4. The power dissipation is limited by 150℃ junctiontemperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D= -250μA	-20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}= -20V, V_{GS}=0V	-	-	-1	μA
I_{GSS}	Gate to Body Leakage Current	V_{DS}=0V, V_{GS}=±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D= -250μA	-0.4	-0.7	-1.0	V
$R_{DS(on)}$	Static Drain-Source on-Resistance note3	V_{GS}= -4.5V, I_D= -10A	-	15.5	21	mΩ
		V_{GS}= -2.5V, I_D= -5A	-	22	30	
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS}= -10V, V_{GS}=0V, f=1.0MHz	-	1840	-	pF
C_{oss}	Output Capacitance		-	151	-	pF
C_{rss}	Reverse Transfer Capacitance		-	58	-	pF
Q_g	Total Gate Charge	V_{DS}= -10V, I_D= -2.3A V_{GS}= -10V	-	3.3	-	nC
Q_{gs}	Gate-Source Charge		-	0.7	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	1.3	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DD}= -15V, I_D= -10A, V_{GS}= -10V, R_{GEN}=3Ω	-	11	-	ns
t_r	Turn-on Rise Time		-	5.5	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	3.5	-	ns
t_f	Turn-off Fall Time		-	4.6	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-30	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-40	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS}=0V, I_S= -10A	-	-	-1.2	V

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: T_J=25℃, V_{DD}=-15V, V_G=-10V, R_G=25Ω, L=0.1mH, I_{AS}= -27A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%

TYPICAL PERFORMANCE CHARACTERISTICS N-CHANNEL

Figure1: Output Characteristics

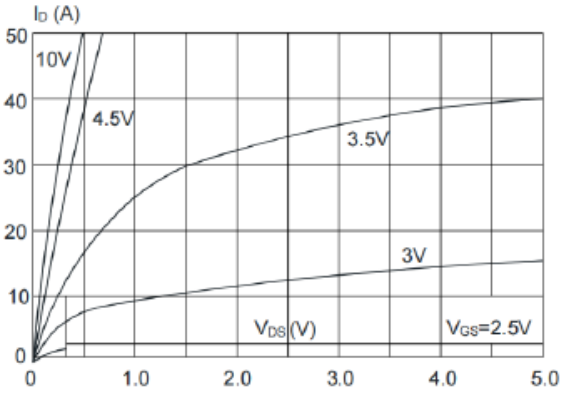


Figure 2: Typical Transfer Characteristics

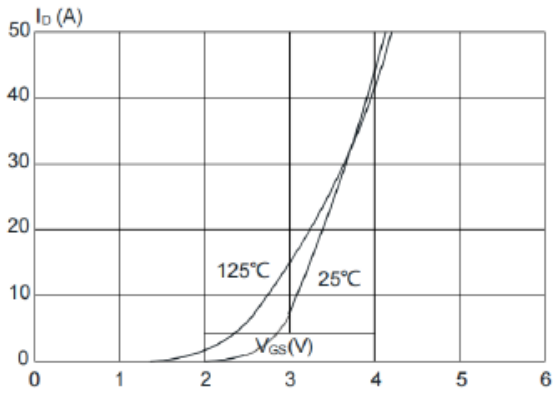


Figure 3: On-resistance vs. Drain Current

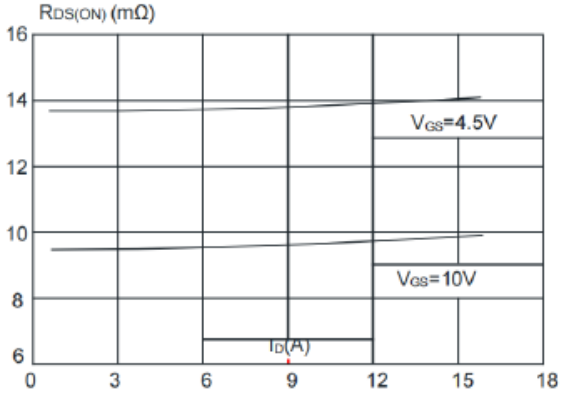


Figure 4: Body Diode Characteristics

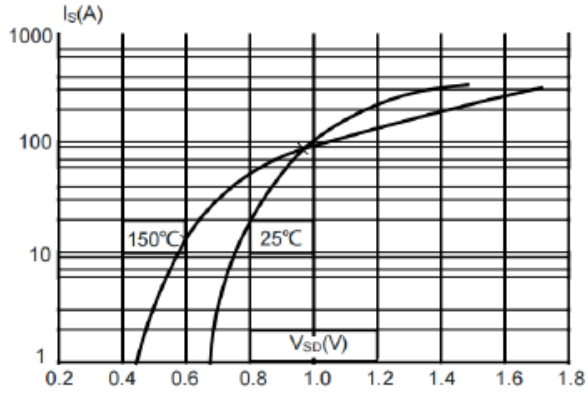


Figure 5: Gate Charge Characteristics

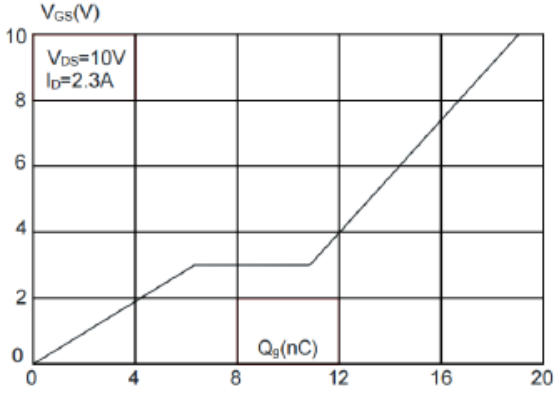
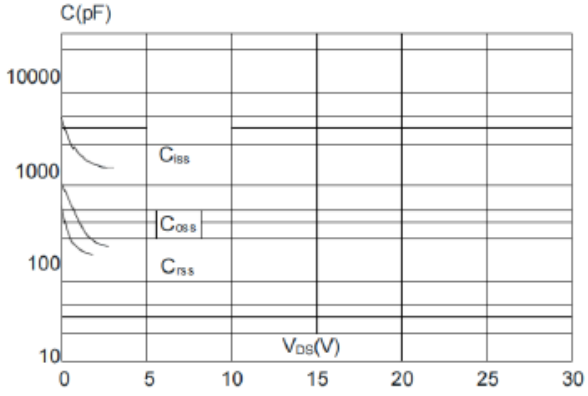


Figure 6: Capacitance Characteristics



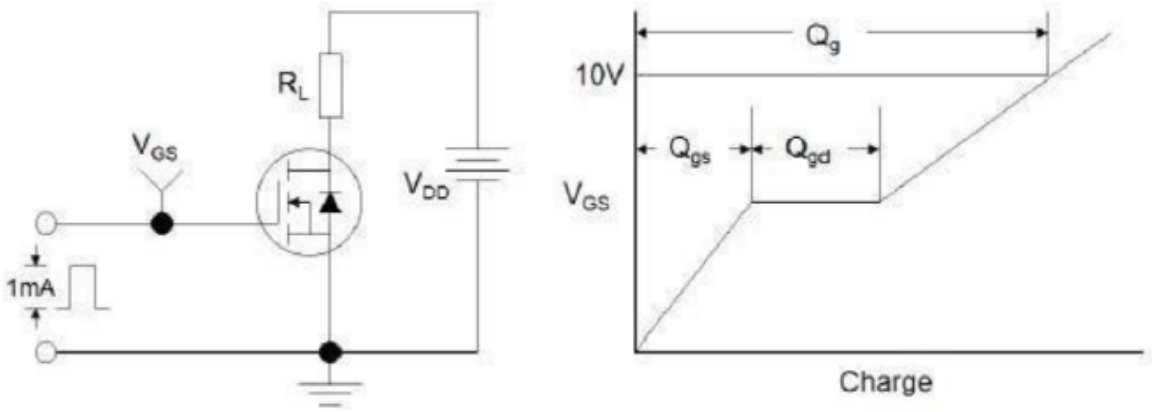


Figure1:Gate Charge Test Circuit & Waveform

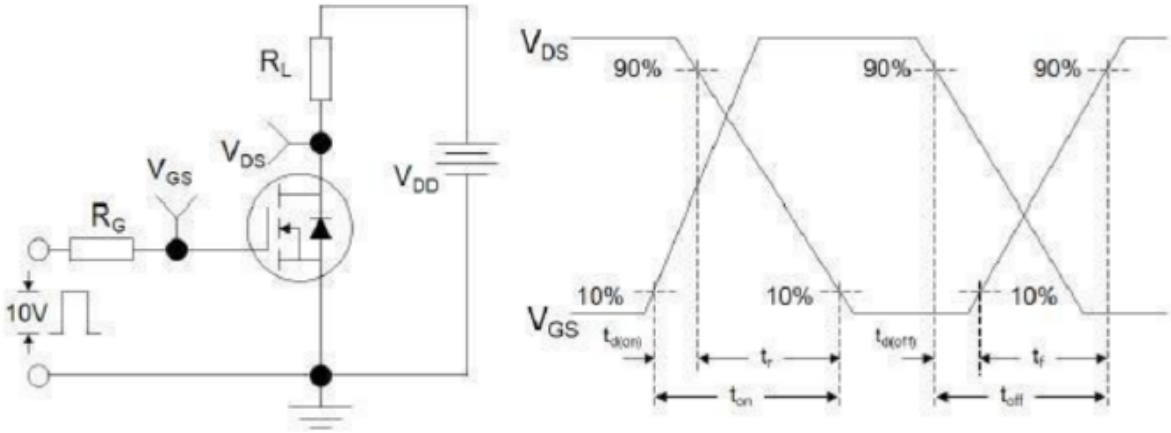


Figure 2: Resistive Switching Test Circuit & Waveforms

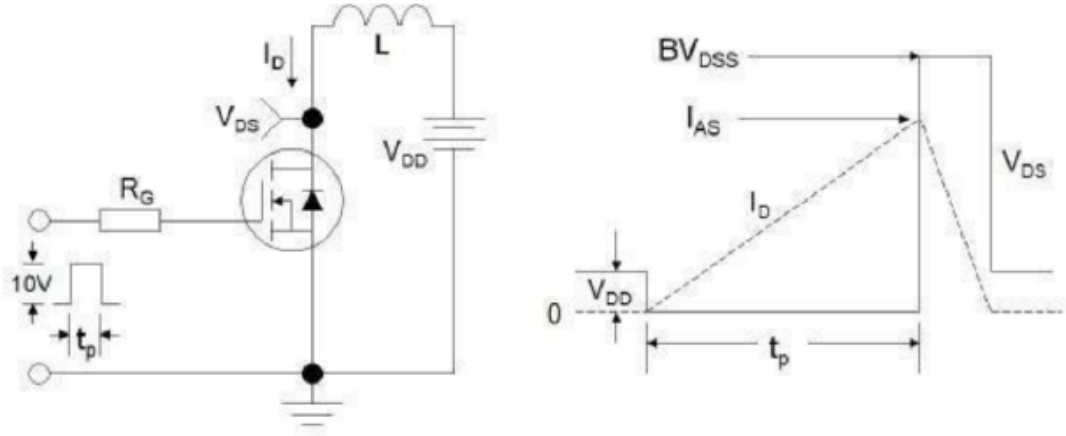


Figure1: Output Characteristics

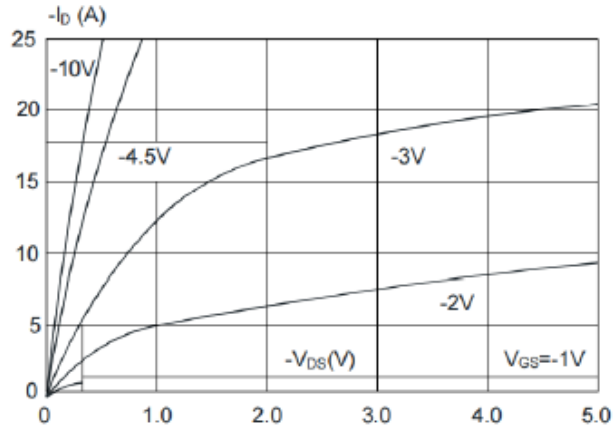


Figure 2: Typical Transfer Characteristics

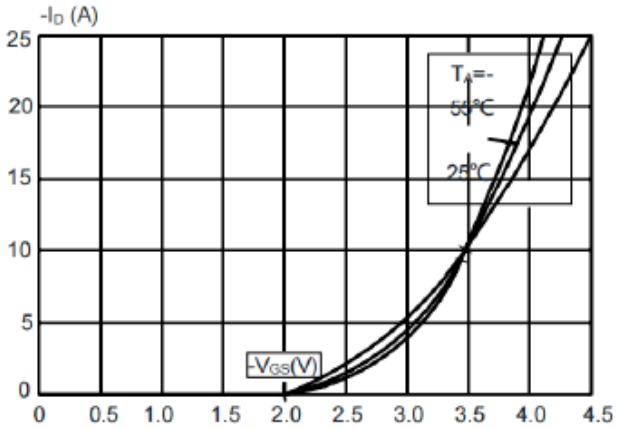


Figure 3: On-resistance vs. Drain Current

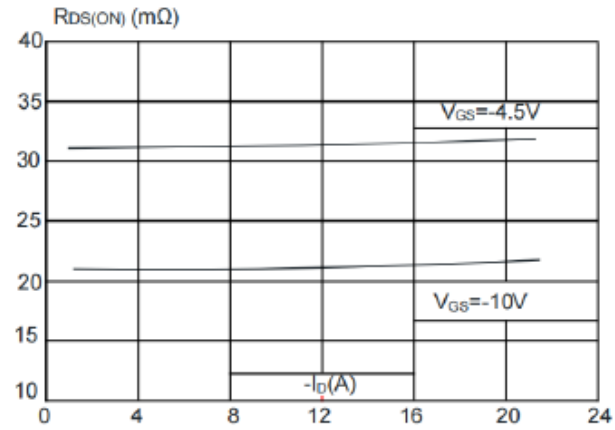


Figure 4: Body Diode Characteristics

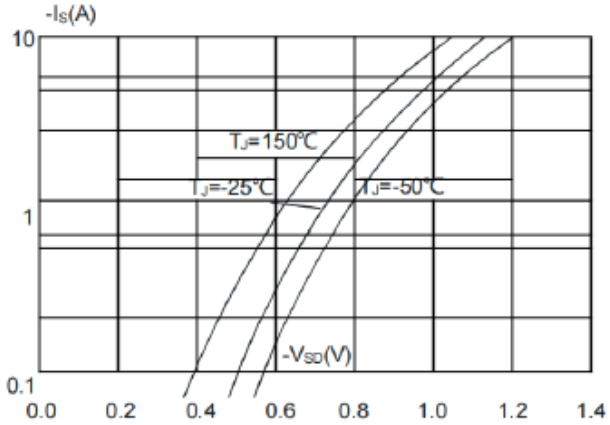


Figure 5: Gate Charge Characteristics

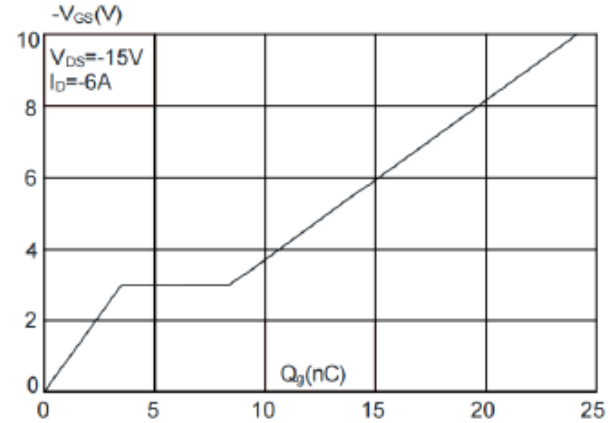


Figure 6: Capacitance Characteristics

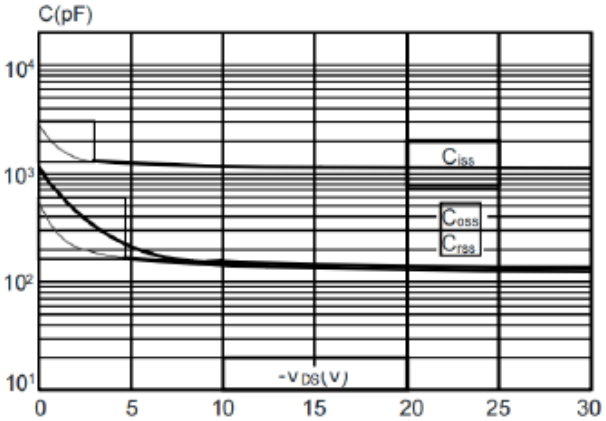


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

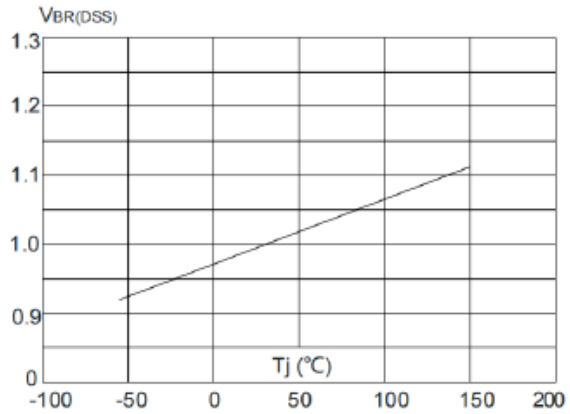


Figure 8: Normalized on Resistance vs. Junction Temperature

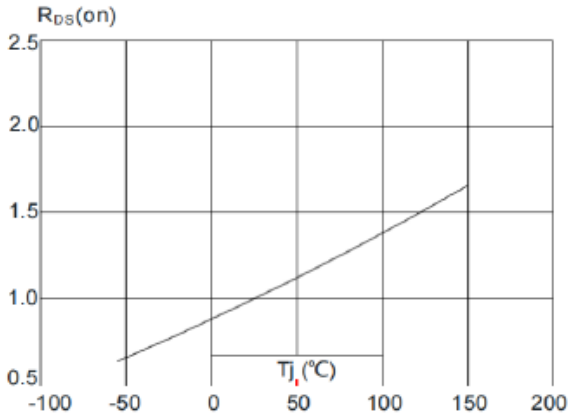


Figure 9: Maximum Safe Operating Area

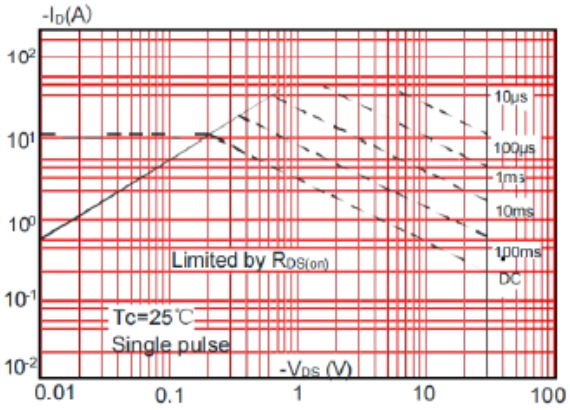


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

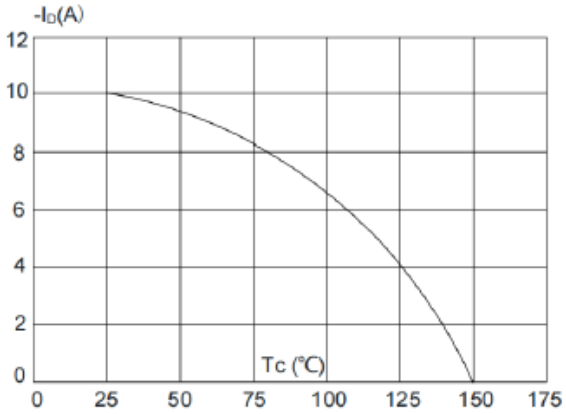
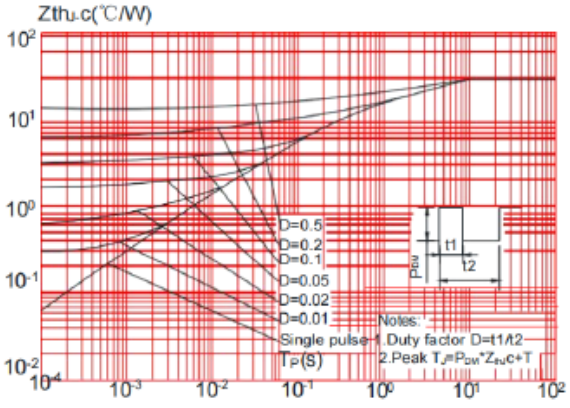
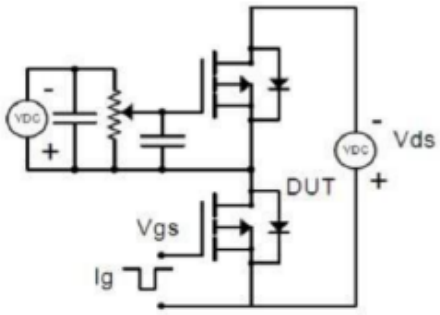
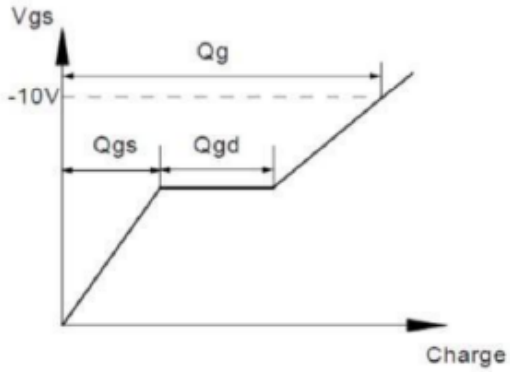


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

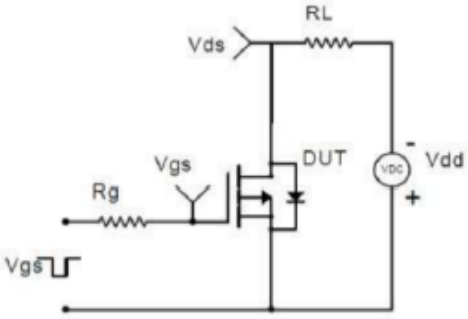


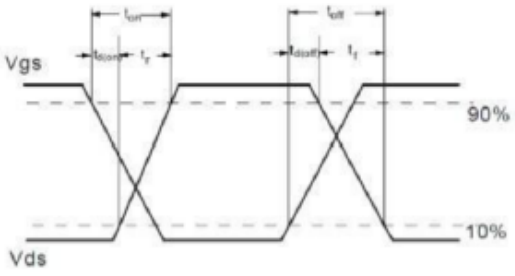
Gate Charge Test Circuit & Waveform



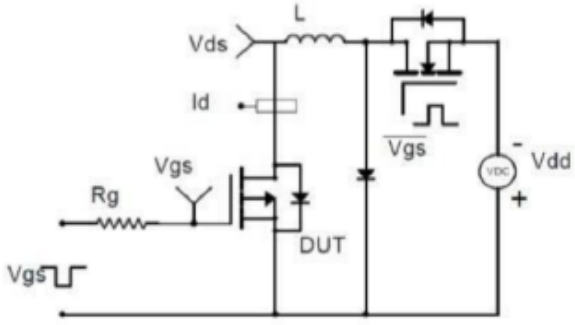


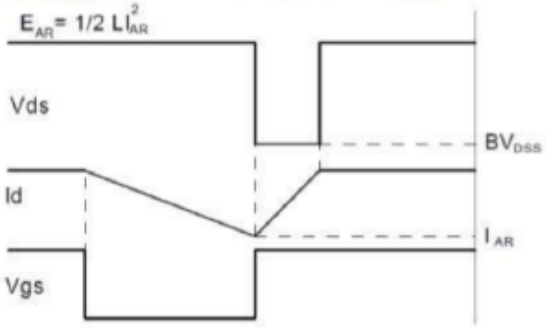
Resistive Switching Test Circuit & Waveforms



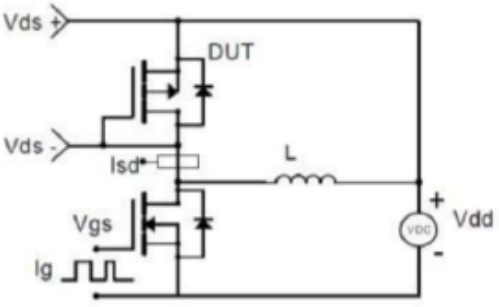


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms



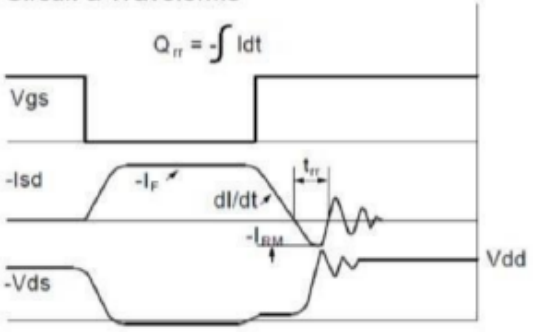


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

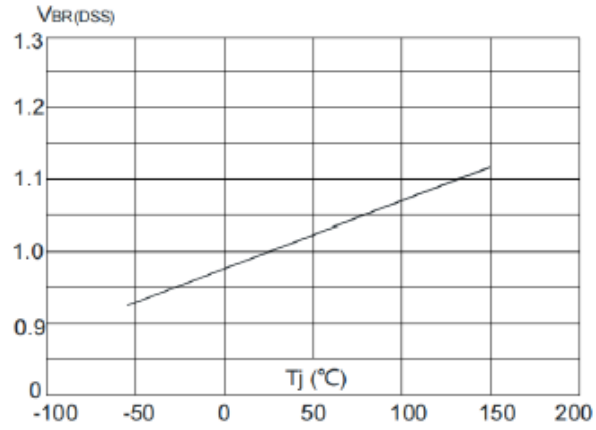


Figure 8: Normalized on Resistance vs. Junction Temperature

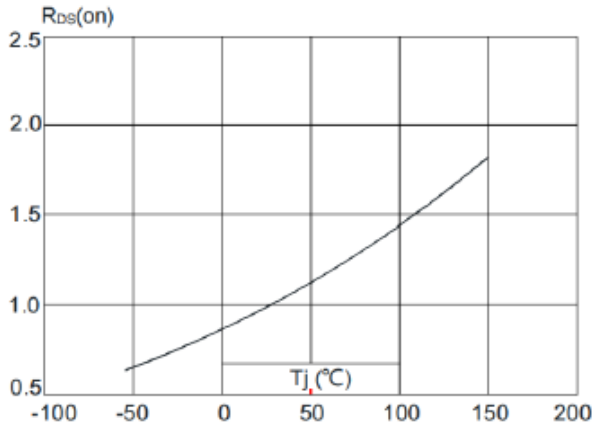


Figure 9: Maximum Safe Operating Area

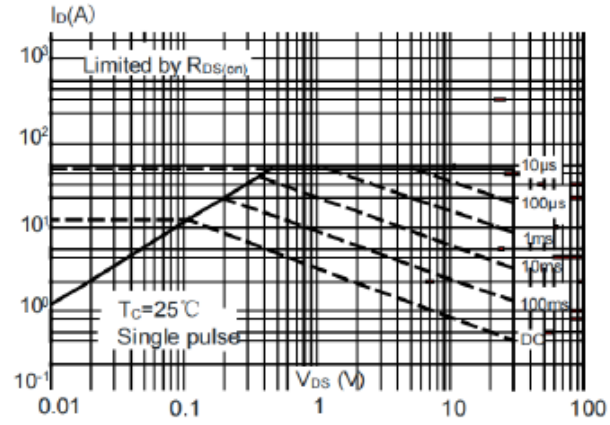


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

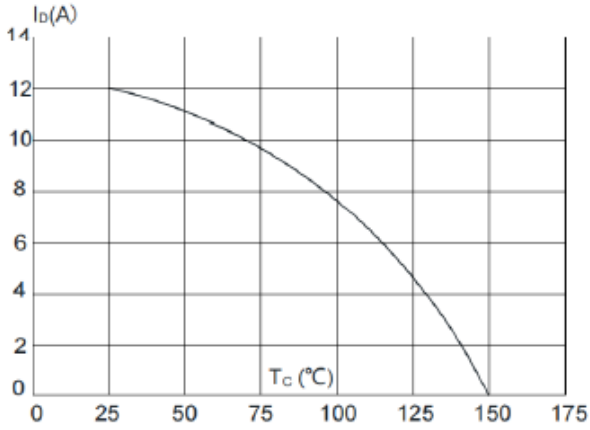
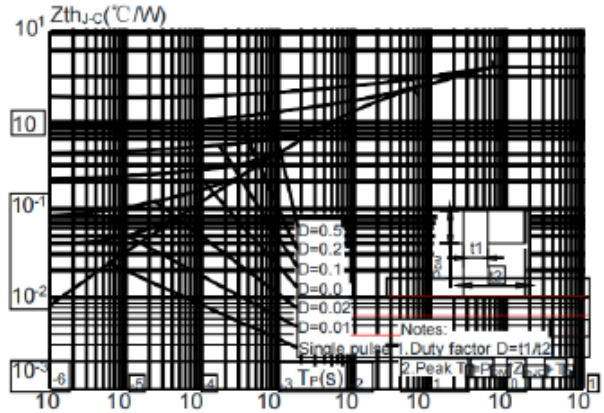
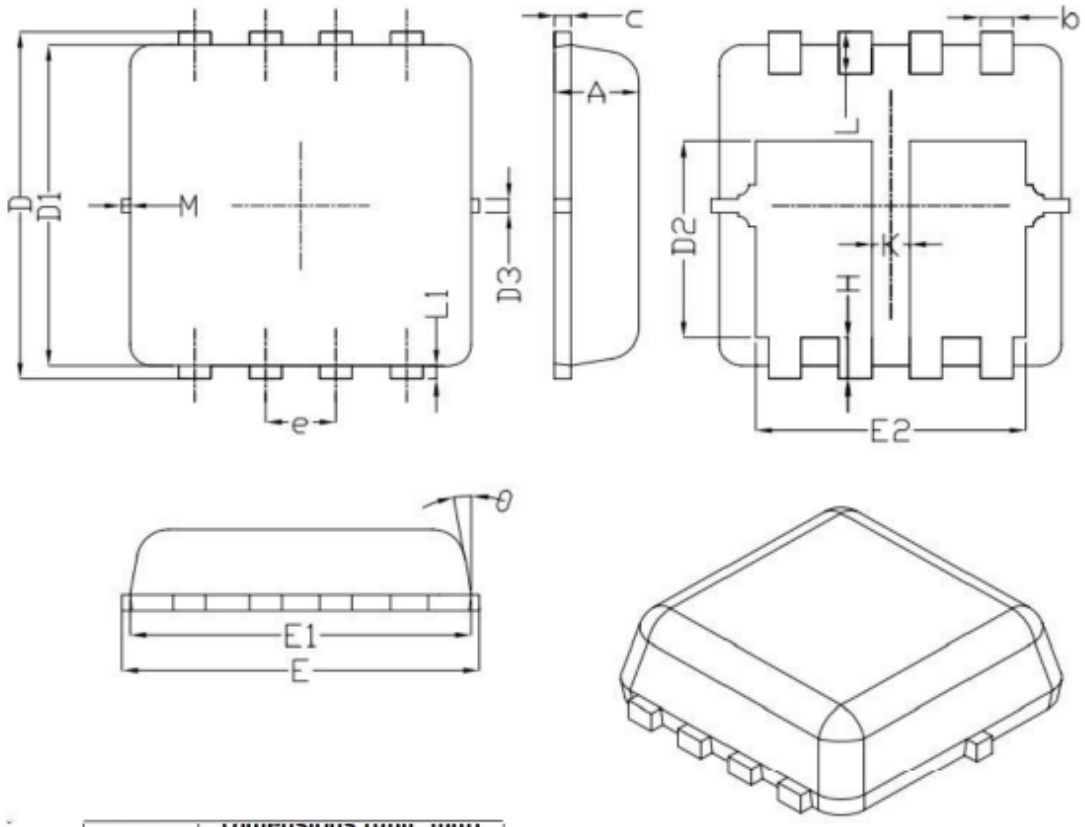


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



Package Mechanical Data-DFN3*3-8L-JQ Single



Symbol	Dimensions (unit: mm)		
	Min	Typ	Max
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	3.25	3.35	3.45
D1	3.00	3.10	3.20
D2	1.78	1.88	1.98
D3	--	0.13	--
E	3.20	3.30	3.40
E1	3.00	3.15	3.20
E2	2.39	2.49	2.59
e	0.65 BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	--	0.13	--
K	0.30	--	--
θ	--	10°	12°
M	*	*	0.15
* Not Specified			

Notes:
1. Refer to JEDEC MO-240 variation CA.
2. Dimensions "D1" and "E1" do NOT include mold flash protrusions or gate burrs.
3. Dimensions "D1" and "E1" include interterminal flash or protrusion.