MY120N10P

100V N-Channel Enhancement Mode MOSFET

MAOYUANWEI semiconductor

General Description

The MY120N10P is silicon N-channel Enhanced VDMOSFETs obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy.

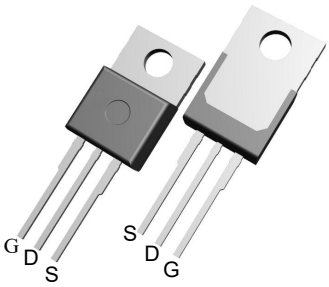
RoHS Compliant

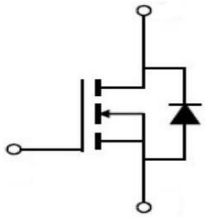
Features

V_{DSS}	100	V
I_D	120	A
P_D(T_C= 2 5 ℃)	215	W
$R_{DS(ON)}$(atV_{GS} = 10V)	5.2	mΩ

Application

- High efficiency switch mode power supplies
- Power factor correction
- Electronic lamp ballast





Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY120N10P	TO-220	MY120N10P	1000

Absolute Maximum Ratings (T_C=25 ℃unless otherwise noted)

Symbol	Parameter		Maximum	Unit
V_{DSS}	Drain-to-Source Voltage		100	V
V_{GSS}	Gate-to-Source Voltage		±25	V
I_D[3]	Continuous Drain Current	T_C=25°C	120	A
		T_C=100°C	97	
I_{DP}[4]	Pulsed Drain Current	T_C=25°C	530	
IAS[5]	Avalanche Current		33	
EAS[5]	Avalanche energy		560	mJ
PD	Maximum Power Dissipation	T_C=25°C	215	W
		T_C=100°C	105	
T_J, T_{STG}	Junction & Storage Temperature Range		-55~175	°C

Thermal Characteristics

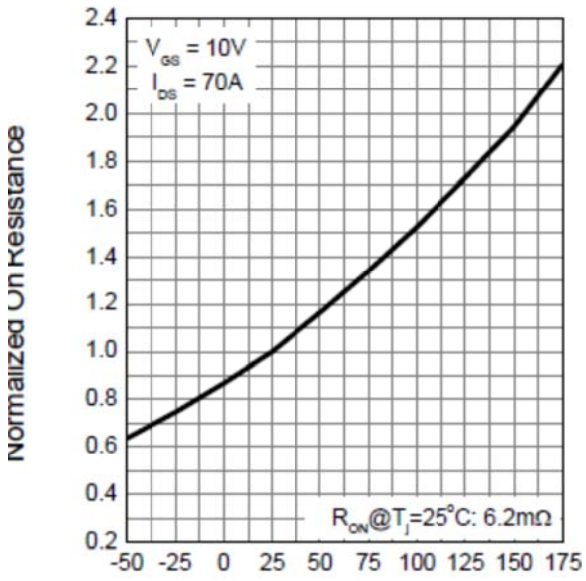
Symbol	Parameter	Typical	Unit
Rθjc	Thermal Resistance-Junction to Case	0.68	℃/W
Rθja	Thermal Resistance-Junction to Ambient	62.5	

Electrical Characteristics (T_C=25 ℃, unless otherwise noted)

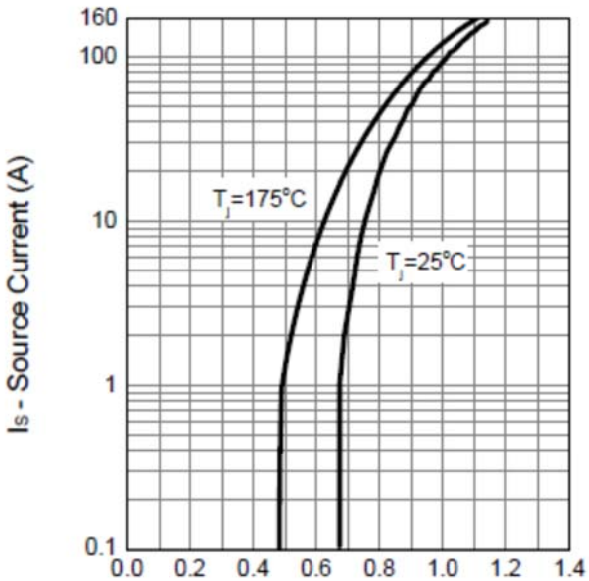
Symbol	Parameter	Test Conditions	Min.	Typ	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V,I_D=250uA	100	—	—	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V,V_{GS}=0V	—	—	1	uA
		T_J=125°C	—	—	20	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250uA	2	3	4	V
I_{GSS}	Gate Leakage Current	V_{GS}=±25V, V_{DS}=0V	—	—	±100	nA
$R_{DS(on)}$[1]	Drain-Source On-Resistance	V_{GS}=10V, I_D=60A	—	5.2	6.2	mΩ
			—	—	—	
Diode Characteristics						
V_{SD}[1]	Diode Forward Voltage	I_{SD}=60A,V_{GS}=0V	—	0.8	1.3	V
I_S[3]	Diode Continuous Forward Current		—	—	50	A
t_{rr}	Reverse Recovery Time	I_F=60A,VDD=50V dI/dt=100A/us	—	65	—	nS
Q_{rr}	Reverse Recovery Charge		—	102	—	nC
Dynamic Characteristics[2]						
R_G	Gate Resistance	V_{GS}=0V, V_{DS}=0V, Frequency=1MHz	—	1.8	—	Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=25V Frequency=1MHz	—	6235	—	pF
C_{oss}	Output Capacitance		—	942	—	
C_{rss}	Reverse Transfer Capacitance		—	506	—	
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=50V,I_D=30A, V_{GS}=10V,R_G=25Ω	—	51	—	nS
t_r	Rise Time		—	116	—	
$t_{d(off)}$	Turn-Off Delay Time		—	247	—	
t_f	Fall Time		—	150	—	
Gate Charge Characteristics[2]						
Q_g	Total Gate Charge	V_{DS}=80V,V_{GS}=10V I_D=30A	—	126.7	—	nC
Q_{gs}	Gate-to-Source Charge		—	20	—	
Q_{gd}	Gate-to-Drain Charge		—	55.5	—	

Note: 1: Pulse test; pulse width ≦ 300us, duty cycle ≦ 2%.
2: Guaranteed by design, not subject to production testing.
3: Package limitation current is 50A.Calculated continuous current based on maximum allowable junction temperature.
4: Repetitive rating, pulse width limited by max junction temperature.
5: Starting TJ = 25°C,L = 0.5mH,VDD=90V. Ias=66A

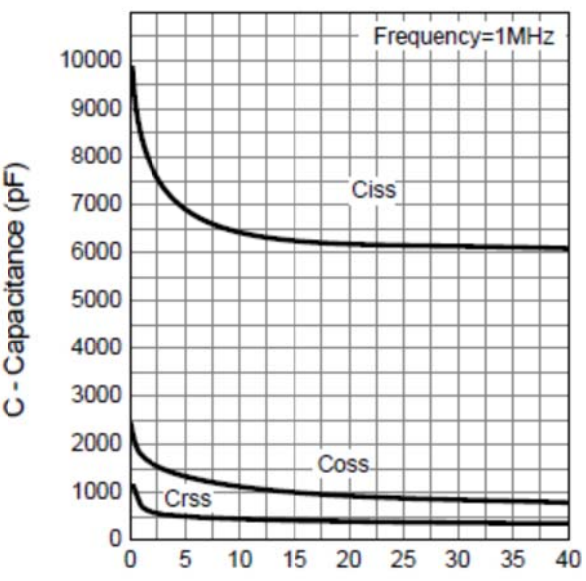
Drain-Source On Resistance



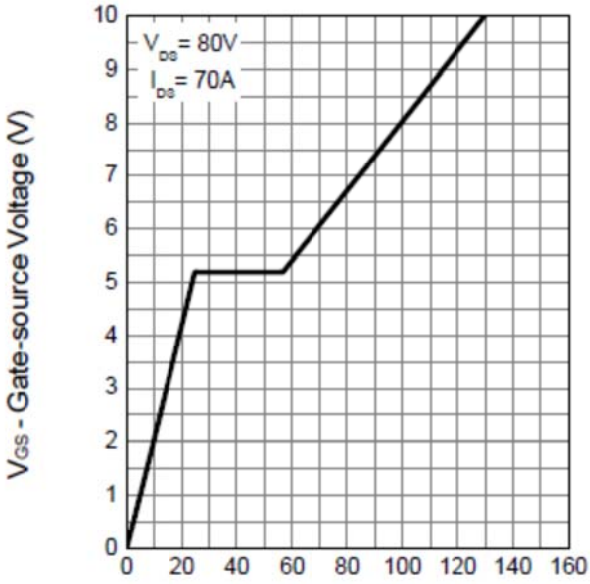
Source-Drain Diode Forward



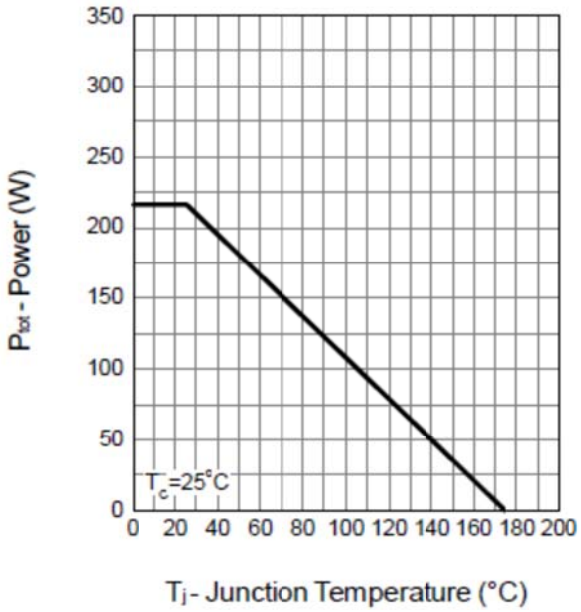
Capacitance



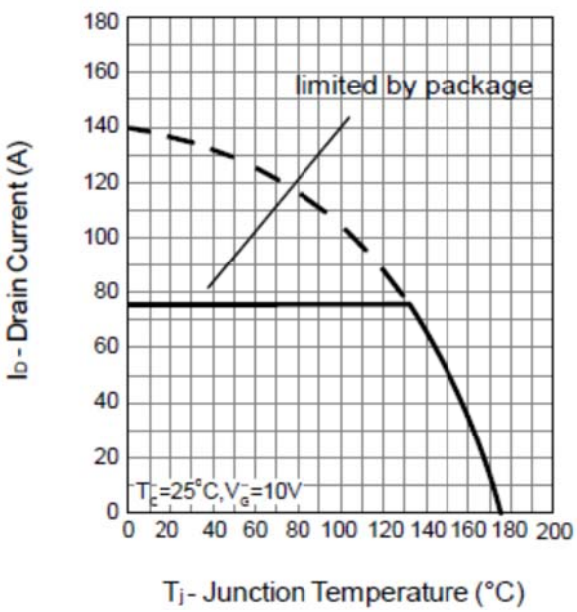
Gate Charge



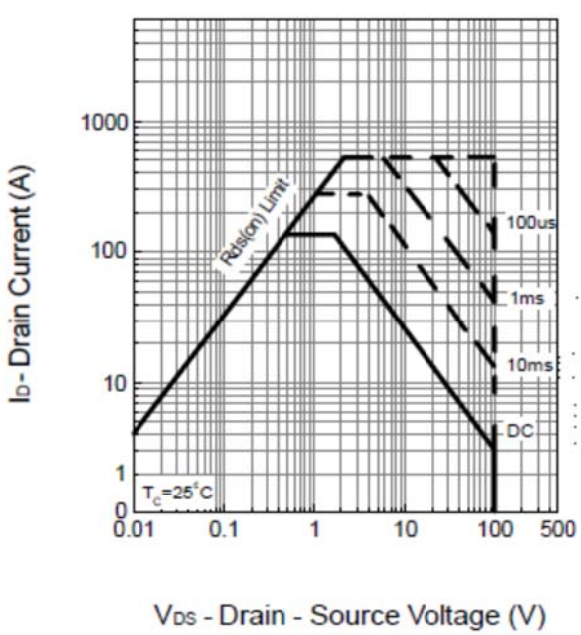
Power Dissipation



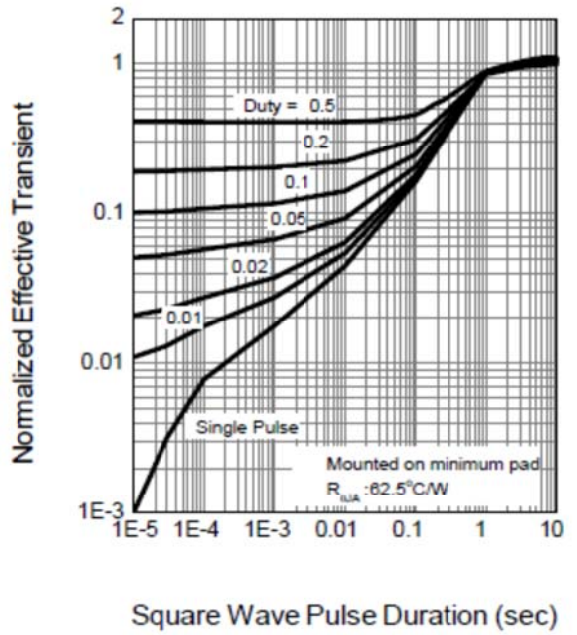
Drain Current



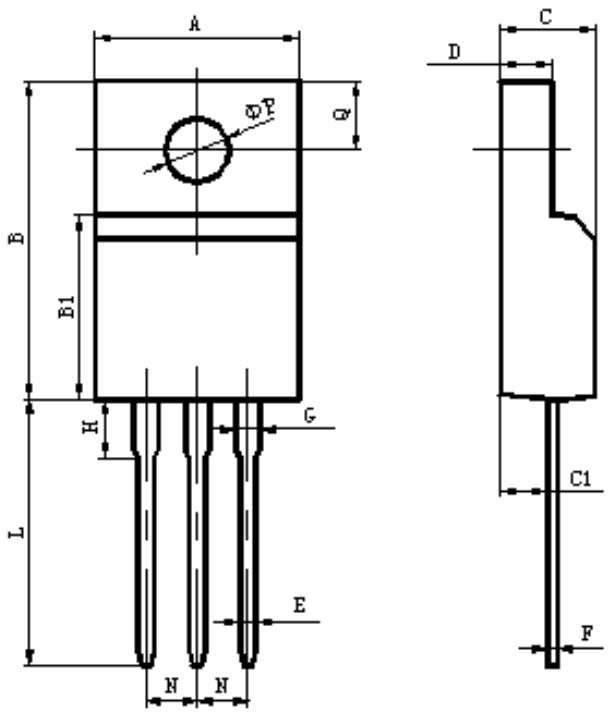
Safe Operation Area



Thermal Transient Impedance



Package Mechanical Data-TO-220 Single



Items	Values(mm)	
	MIN	MAX
A	9.60	10.4
B	15.4	16.2
B1	8.90	9.50
C	4.30	4.90
C1	2.10	3.00
D	2.40	3.00
E	0.60	1.00
F	0.30	0.60
G	1.12	1.42
H	3.40	3.80
	2.40	2.90
L*	12.0	14.0
N	2.34	2.74
Q	3.15	3.55
Φ P	2.90	3.30