

General Description

The MY10N10C use advanced SGT MOSFET technology to provide low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics. This device is specially designed to get better ruggedness and suitable

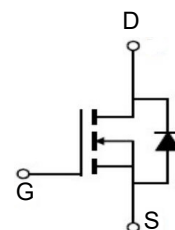
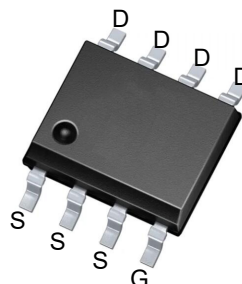


Features

V_{DSS}	100	V
I_D	10	A
$P_D(T_A=25^{\circ}C)$	3.5	W
$R_{DS(ON)}(at V_{GS}=4.5V)$	<18	m Ω

Application

- Consumer electronic power supply
- Motor control
- Synchronous-rectification
- Isolated DC
- Synchronous-rectification applications



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY10N10C	SOP-8	018IN	3000

Absolute Maximum Ratings ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	100	V
Gate source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾	I_D	10	A
Pulsed drain current ²⁾	I_D , pulse	30	A
Power dissipation ³⁾	P_D	3.5	W
Single pulsed avalanche energy ⁵⁾	EAS	30	mJ
Operation and storage temperature	T_{stg} , T_j	-55 to 150	$^{\circ}C$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal resistance, junction-ambient ⁴⁾	$R_{\theta JA}$	35.7	$^{\circ}C/W$

Max.

Electrical Characteristics ($T_J=25\text{ }^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	100			V	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	1.0		2.5	V	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$
Drain-source on-state resistance	$R_{DS(on)}$			18	$\text{m}\Omega$	$V_{GS}=10\text{ V}$, $I_D=8\text{ A}$
Drain-source on-state resistance	$R_{DS(on)}$			26	$\text{m}\Omega$	$V_{GS}=4.5\text{ V}$, $I_D=6\text{ A}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=20\text{ V}$
				-100		$V_{GS}=-20\text{ V}$
Drain-source leakage current	I_{DSS}			1	μA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$
Input capacitance	C_{iss}		1190.6		pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}		194.6		pF	
Reverse transfer capacitance	C_{rss}		4.1		pF	
Turn-on delay time	$t_{d(on)}$		17.8		ns	$V_{GS}=10\text{ V}$, $V_{DS}=50\text{ V}$, $R_G=2.2\text{ }\Omega$, $I_D=10\text{ A}$
Rise time	t_r		3.9		ns	
Turn-off delay time	$t_{d(off)}$		33.5		ns	
Fall time	t_f		3.2		ns	
Total gate charge	Q_g		19.8		nC	$I_D=8\text{ A}$, $V_{DS}=50\text{ V}$, $V_{GS}=10\text{ V}$
Gate-source charge	Q_{gs}		2.4		nC	
Gate-drain charge	Q_{gd}		5.3		nC	
Gate plateau voltage	$V_{plateau}$		3.2		V	
Diode forward current	I_S			8	A	$V_{GS}<V_{th}$
Pulsed source current	I_{SP}			32		
Diode forward voltage	V_{SD}			1.3	V	$I_S=8\text{ A}$, $V_{GS}=0\text{ V}$
Reverse recovery time	t_{rr}		50.2		ns	$I_S=8\text{ A}$, $di/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}		95.1		nC	
Peak reverse recovery current	I_{rrm}		2.5		A	

Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a=25\text{ }^{\circ}\text{C}$.
- 5) $V_{DD}=50\text{ V}$, $R_G=25\text{ }\Omega$, $L=0.3\text{ mH}$, starting $T_J=25\text{ }^{\circ}\text{C}$.

Typical Characteristics

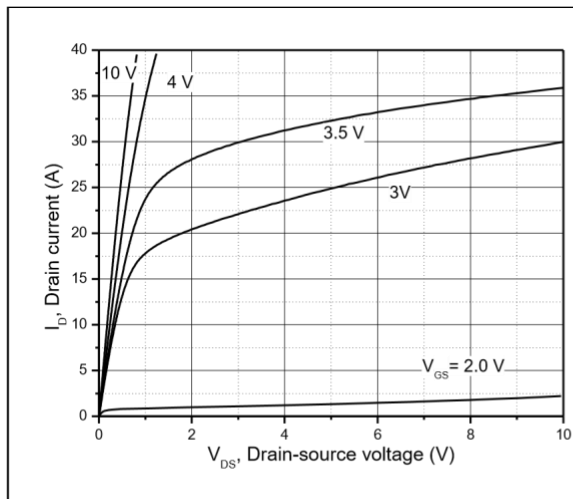


Figure 1, Typ. output characteristics

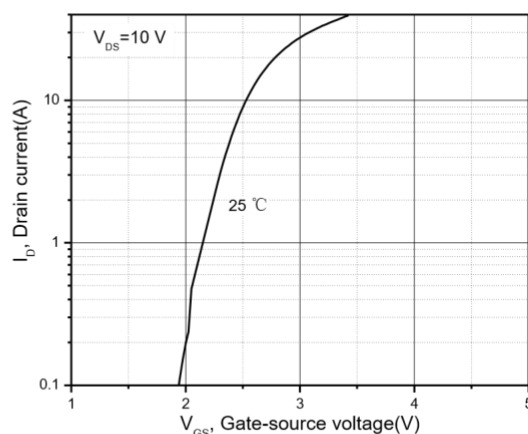


Figure 2, Typ. transfer characteristics

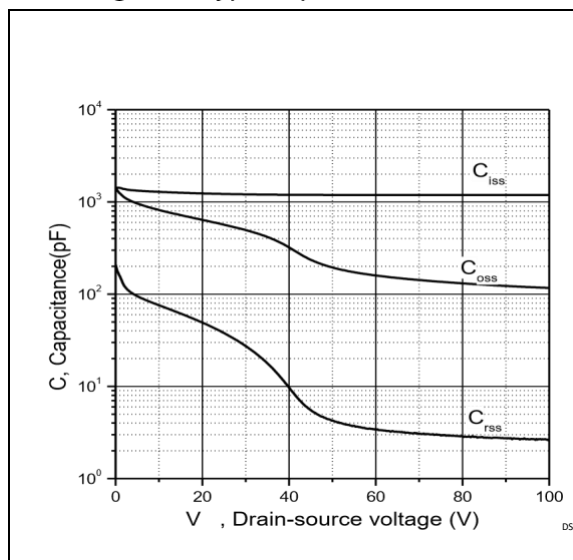


Figure 3, Typ. capacitances

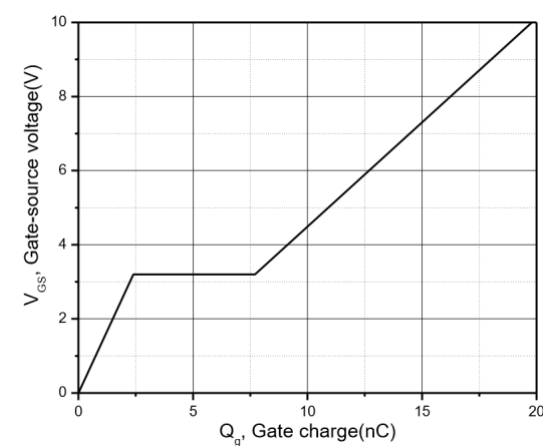


Figure 4, Typ. gate charge

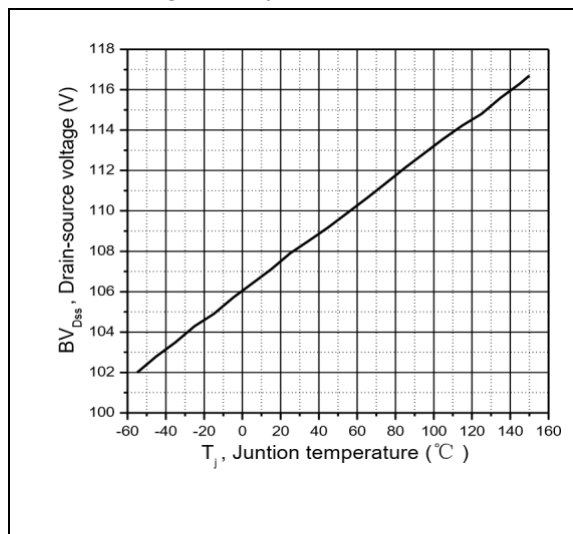


Figure 5, Drain-source breakdown voltage

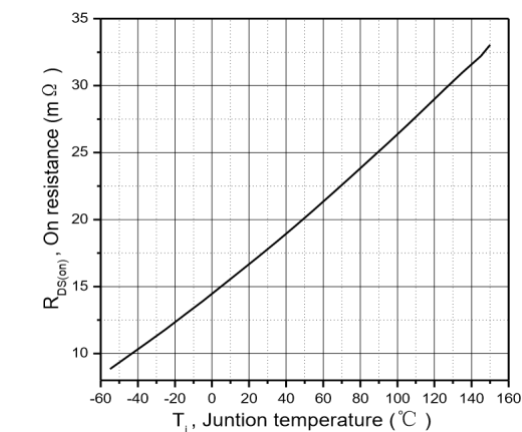


Figure 6, Drain-source on-state resistance

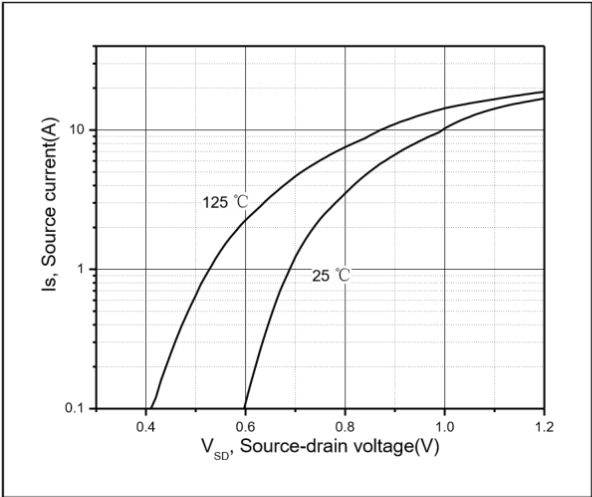


Figure 7, Forward characteristic of body diode

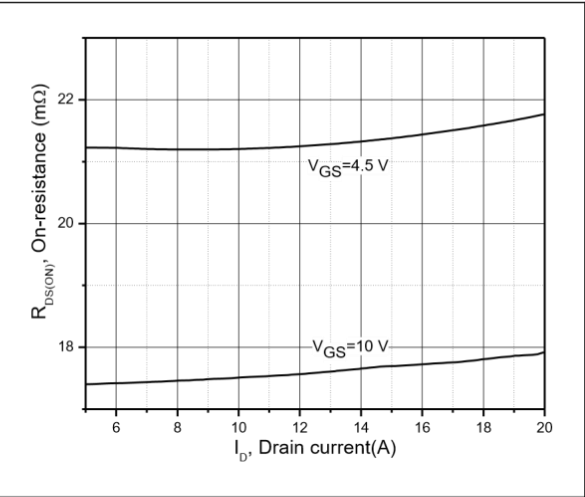


Figure 8, Drain-source on-state resistance

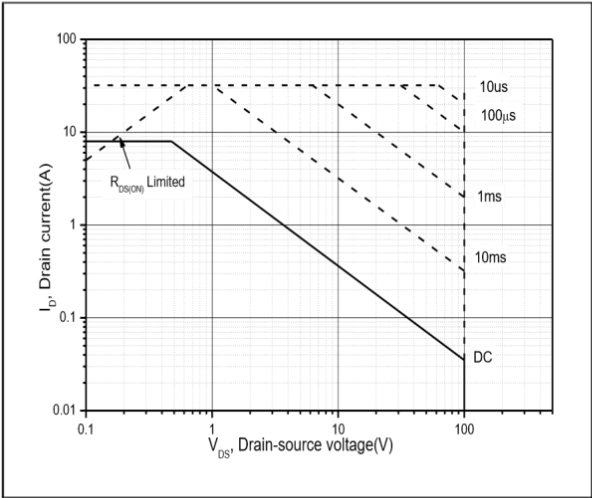


Figure 9, Safe operation area T_C=25 °C

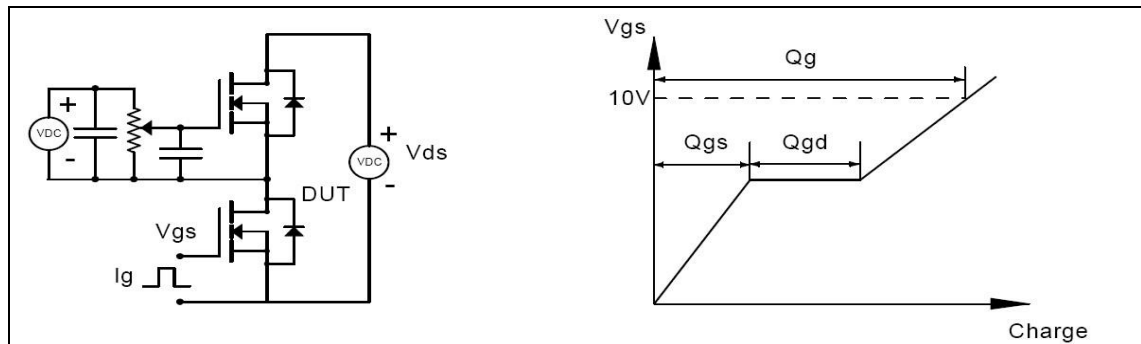


Figure 1, Gate charge test circuit & waveform

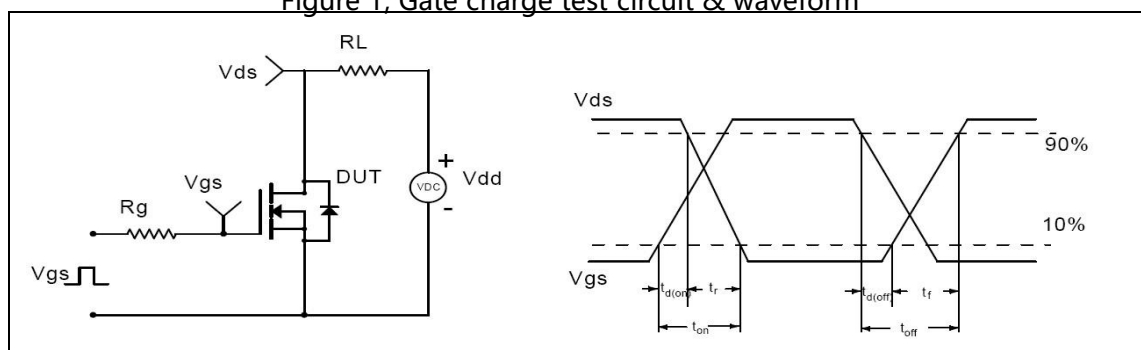


Figure 2, Switching time test circuit & waveforms

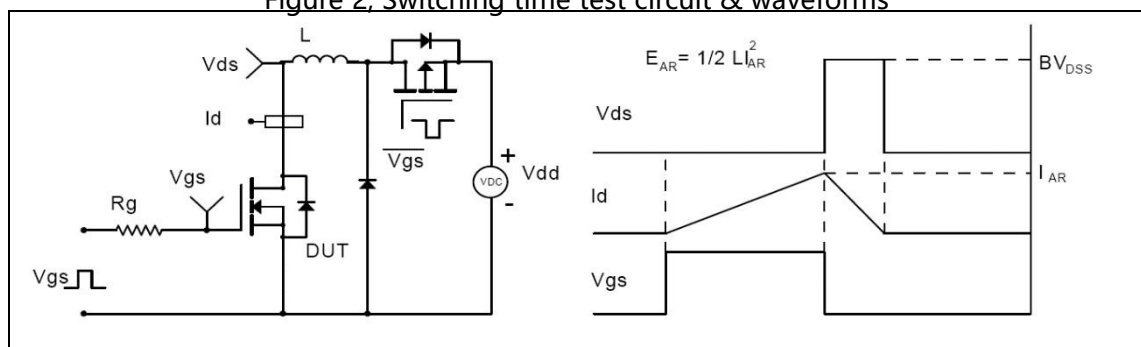


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

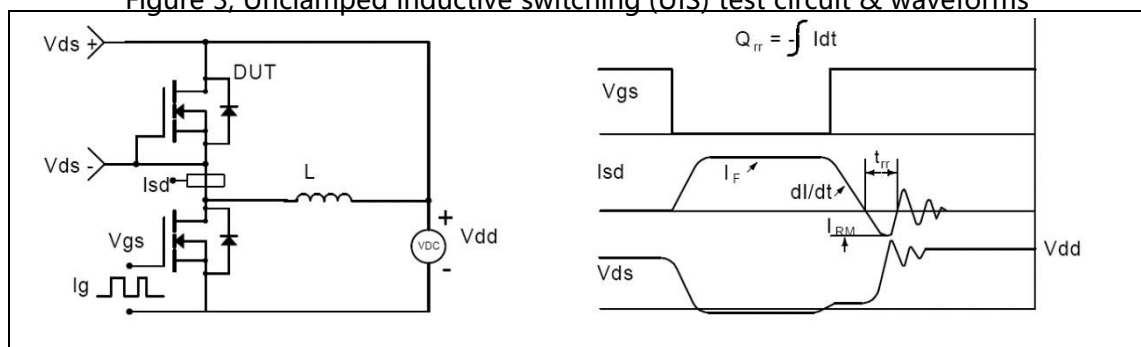


Figure 4, Diode reverse recovery test circuit & waveforms

Package Mechanical Data-SOP-8

