

General Description

The MY040FNC uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

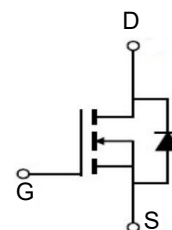
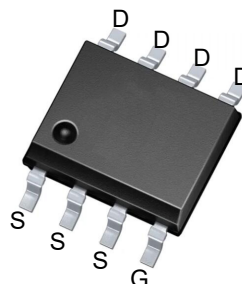


Features

V_{DSS}	60	V
I_D	6.5	A
$R_{DS(ON)}(at V_{GS}=10V)$	<37	m Ω
$R_{DS(ON)}(at V_{GS}=4.5V)$	<48	m Ω

Application

- Battery protection
- Load switch
- Uninterruptible power supply



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
MY040FNC	SOP-8	040FNC	3000

Absolute Maximum Ratings ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_A=25^{\circ}\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	6.5	A
$I_D@T_A=70^{\circ}\text{C}$	Continuous Drain Current, $V_{GS} @ 10V^1$	5.5	A
I_{DM}	Pulsed Drain Current ²	18	A
EAS	Single Pulse Avalanche Energy ³	22	mJ
I_{AS}	Avalanche Current	21	A
$P_D@T_A=25^{\circ}\text{C}$	Total Power Dissipation ⁴	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^{\circ}\text{C}$
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	85	$^{\circ}\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	25	$^{\circ}\text{C/W}$

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1mA$	---	0.044	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=4A$	---	28	37	$m\Omega$
		$V_{GS}=4.5V, I_D=2A$	---	35	48	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	1.6	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.8	---	$mV/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=48V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=48V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=4A$	---	28.3	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1MHz$	---	2.5	---	
Q_g	Total Gate Charge (10V)	$V_{DS}=48V, V_{GS}=10V, I_D=4A$	---	19	---	nC
Q_{gs}	Gate-Source Charge		---	2.6	---	
Q_{gd}	Gate-Drain Charge		---	4.1	---	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=30V, V_{GS}=10V, R_G=3.3\Omega, I_D=4A$	---	3	---	ns
T_r	Rise Time		---	34	---	
$T_{d(off)}$	Turn-Off Delay Time		---	23	---	
T_f	Fall Time		---	6	---	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1MHz$	---	1027	---	pF
C_{oss}	Output Capacitance		---	65	---	
C_{rss}	Reverse Transfer Capacitance		---	46	---	
I_S	Continuous Source Current ^{1,5}	$V_G=V_D=0V, \text{Force Current}$	---	---	4.5	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	18	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=4A, di/dt=100A/\mu s,$	---	12.1	---	nS
Q_{rr}	Reverse Recovery Charge		---	6.7	---	nC

Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
2. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=21A$
4. The power dissipation is limited by 150°C junction temperature 5 .The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

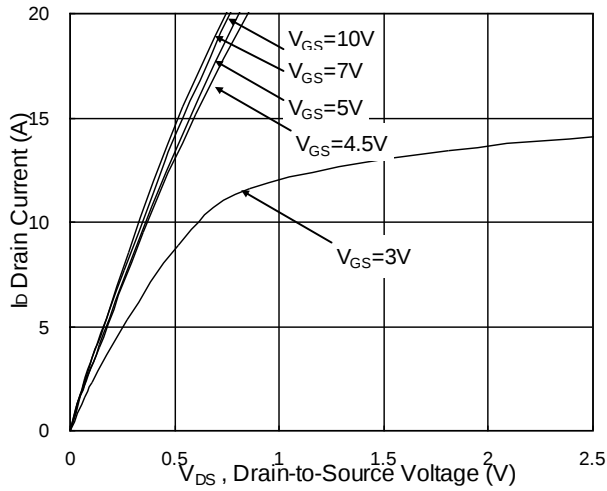


Fig.1 Typical Output Characteristics

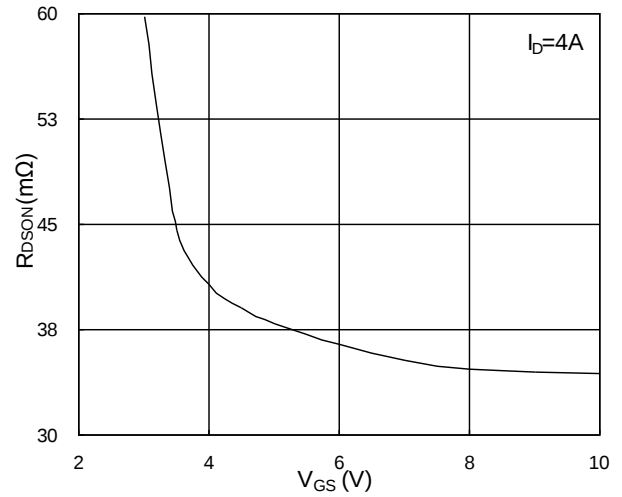


Fig.2 On-Resistance vs. Gate-Source

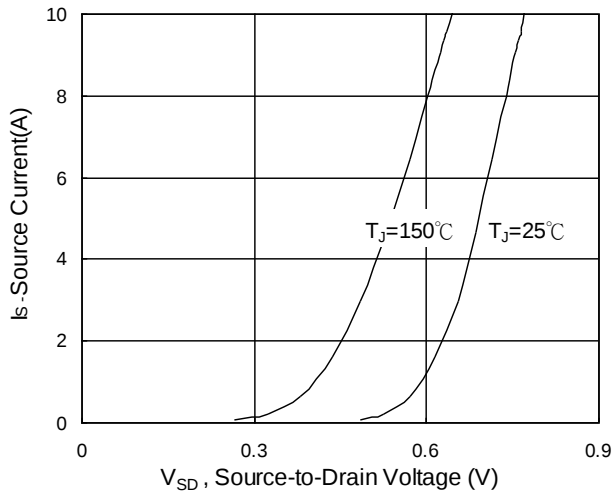


Fig.3 Forward Characteristics Of Reverse

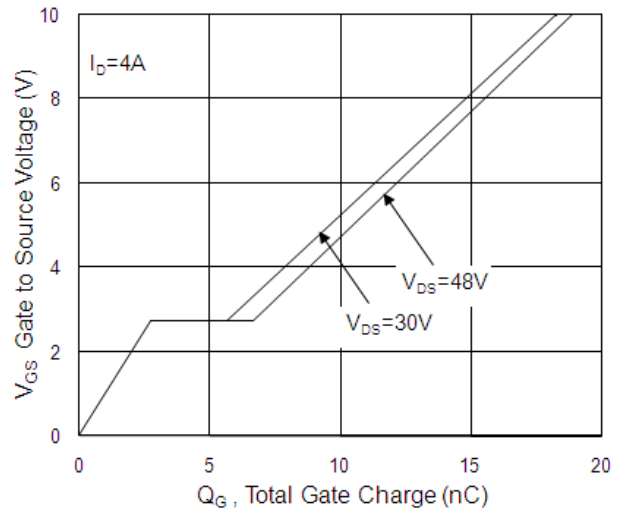


Fig.4 Gate-Charge Characteristics

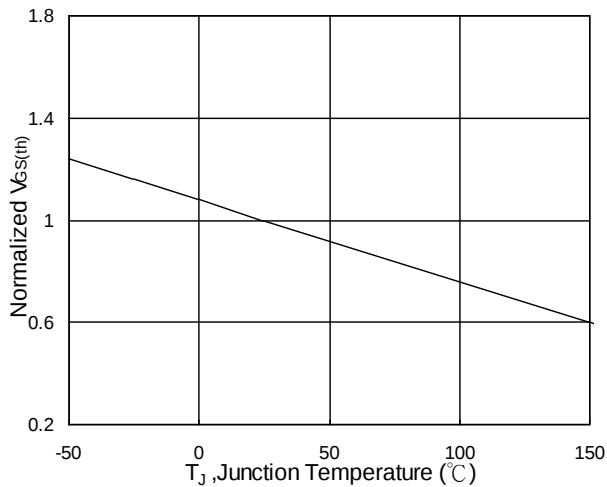


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

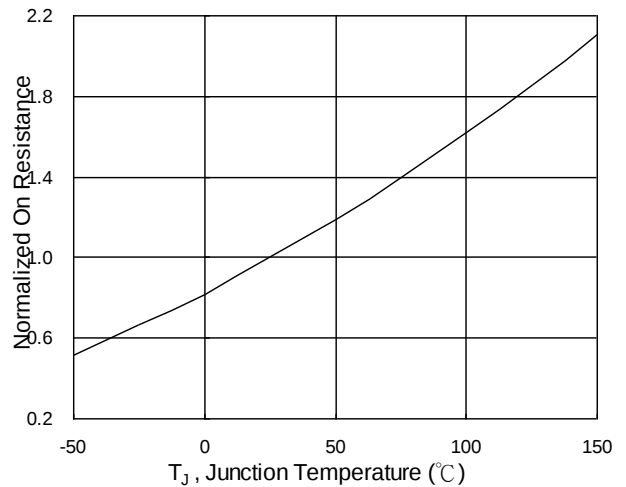


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

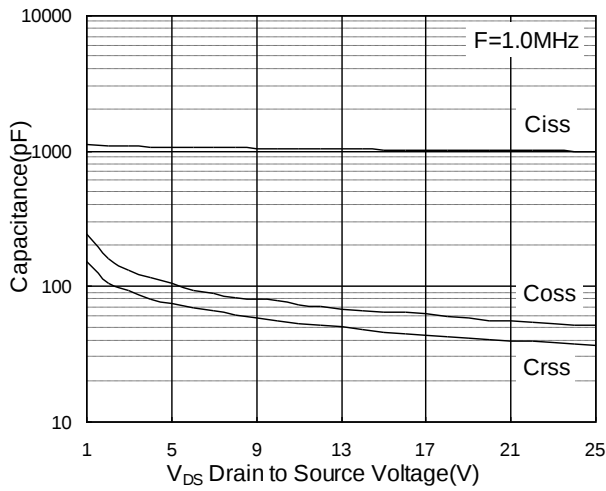


Fig.7 Capacitance

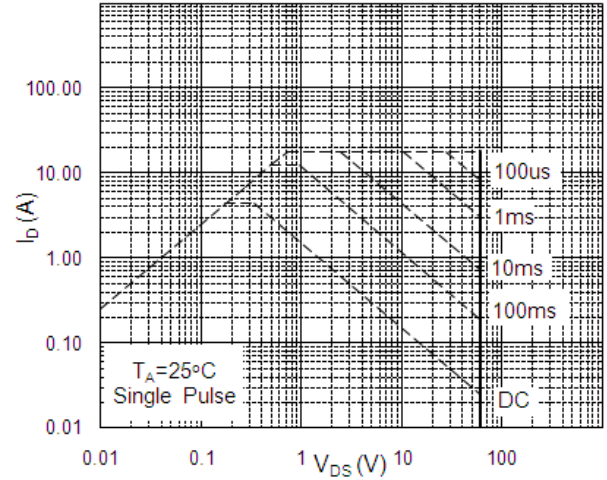


Fig.8 Safe Operating Area

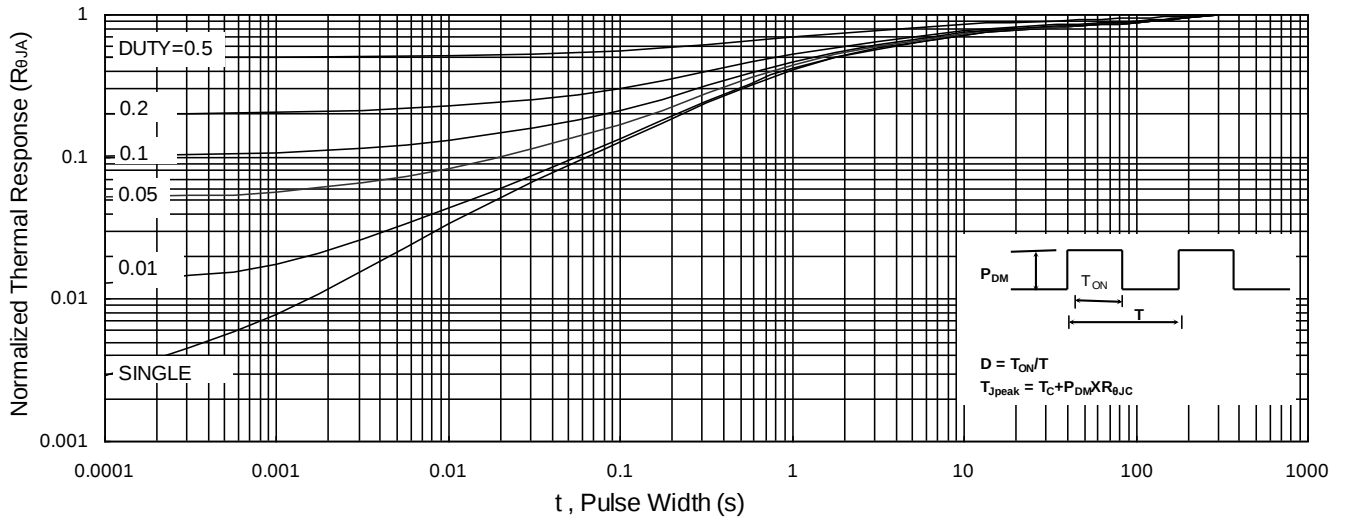


Fig.9 Normalized Maximum Transient Thermal Impedance

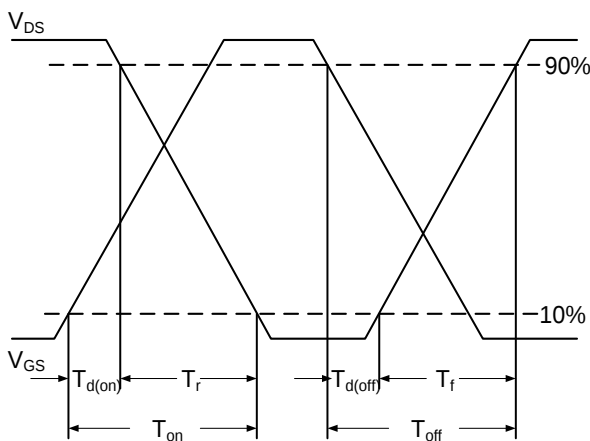


Fig.10 Switching Time Waveform

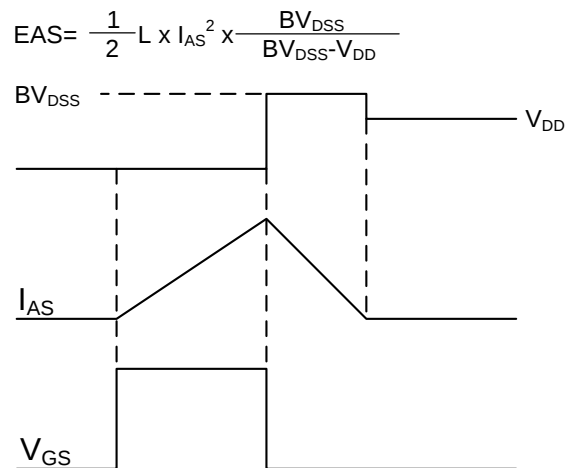
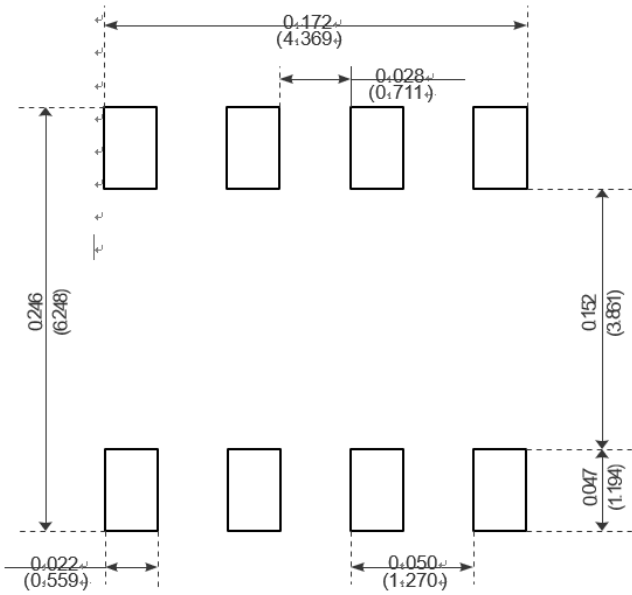
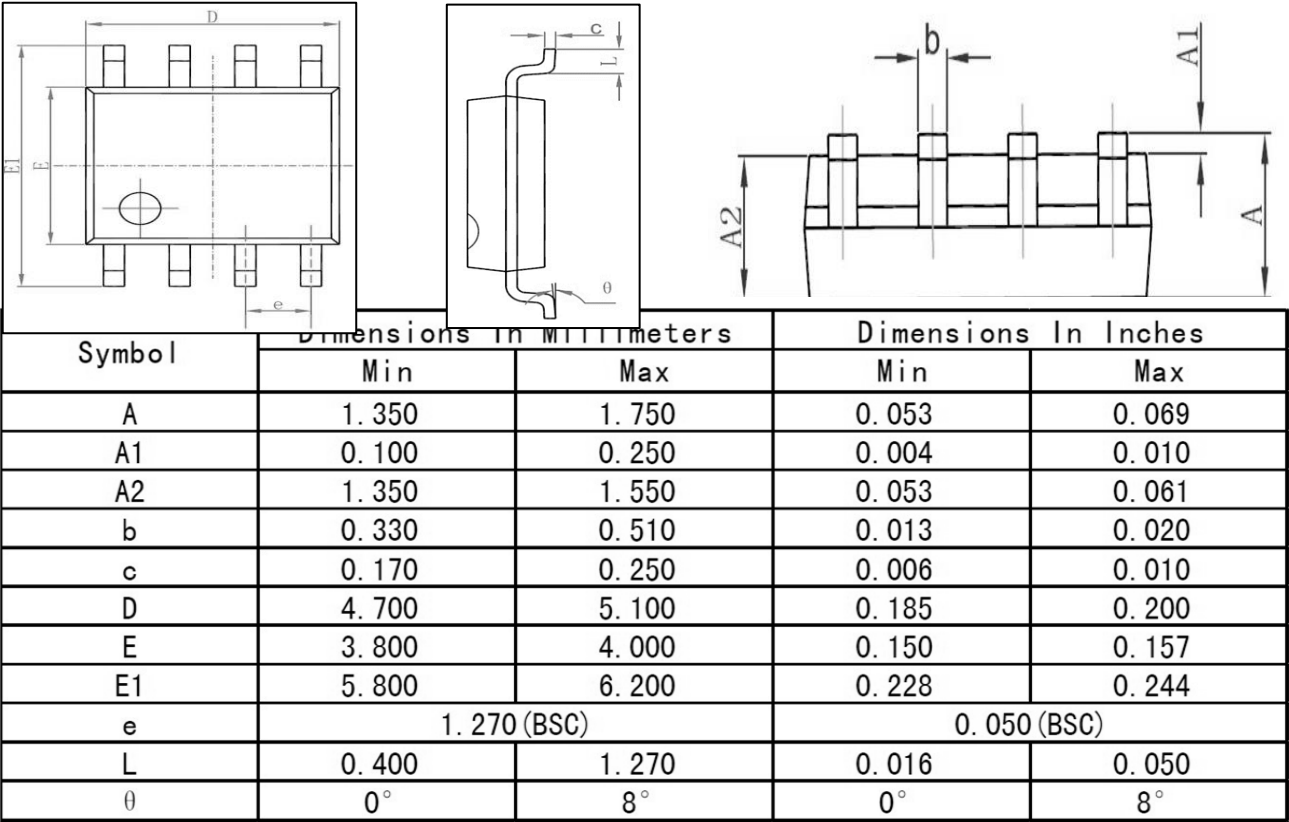


Fig.11 Unclamped Inductive Switching Waveform

Package Mechanical Data-SOP-8



Recommended Minimum Pads