AP80P06NF

-60V P-Channel Enhancement ModeMOSFET

MAOYUANWEI semiconductor

General Description

The AP80P06NF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a load switch or in PWM applications.

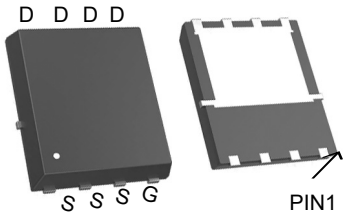
RoHS Compliant

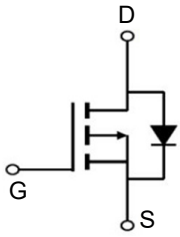
Features

V_{DSS}	-60	V
I_D	-80	A
$R_{DS(ON)}$(atV_{GS} =-10V)	13	mÝ
$R_{DS(ON)}$(atV_{GS} =-4.5V)	16	mÝ

Application

- PWM applications
- Load switch
- Power management





Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP80P06NF	PDFN5*6-8L	80P06	5000

Absolute Maximum Ratings (T_A=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous@ Current-Pulsed (Note 1)	I_D(25℃)	-80	A
	I_D(70℃)	-50	A
	I_{DM}	-85	A
Maximum Power Dissipation	P_D	60	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 175	℃
Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	25	℃/W

Electrical Characteristics (T_A=25 ℃, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=-250μA	-60			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-48V,V_{GS}=0V			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250μA	-1	-1.8	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-20A		13	17	mΩ
		V_{GS}=-4.5V, I_D=-20A		16	20	mΩ
Forward Transconductance	g_{FS}	V_{DS}=-5V,I_D=-20A	5			S
Input Capacitance	C_{lss}	V_{DS}=-30V,V_{GS}=0V, F=1.0MHz		4130		PF
Output Capacitance	C_{oss}			420		PF
Reverse Transfer Capacitance	C_{rss}			145		PF
Turn-on Delay Time	$t_{d(on)}$	V_{DS}=-30V,V_{GS}=-10V,R_{GEN}=3Ω I_D=1A		14		nS
Turn-on Rise Time	t_r			20		nS
Turn-Off Delay Time	$t_{d(off)}$			40		nS
Turn-Off Fall Time	t_f			19		nS
Total Gate Charge	Q_g	V_{DS}=-30V,I_D=-20A,V_{GS}=-10V		48		nC
Gate-Source Charge	Q_{gs}			11		nC
Gate-Drain Charge	Q_{gd}			10		nC
Body Diode Reverse Recovery Time	T_{rr}	I_F=-20A, dI/dt=100A/μs		40		nS
Body Diode Reverse Recovery Charge	Q_{rr}			56		nC
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=-1A		-0.72	-1	V

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on 1in^2 FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%. **4.** Guaranteed by design, not subject to production testing.

Typical Characteristics

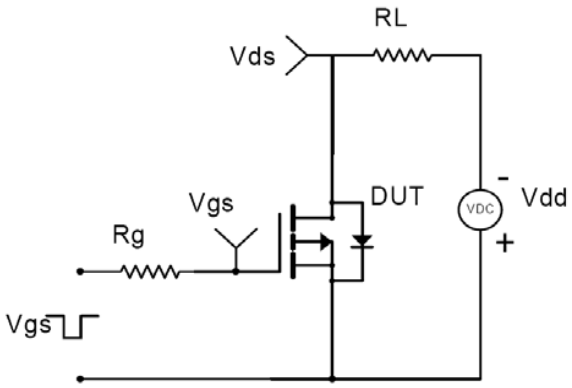


Figure 1:Switching Test Circuit

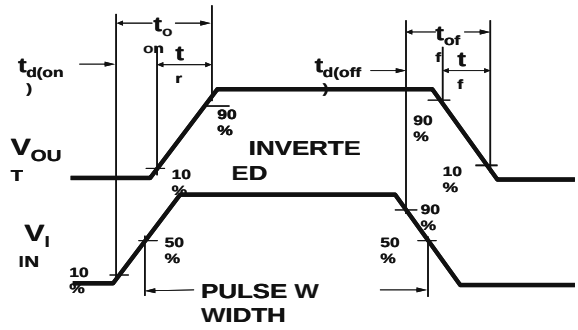


Figure 2:Switching Waveforms

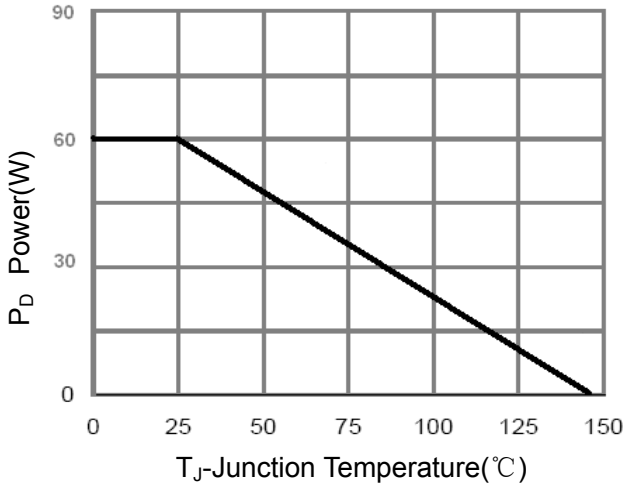


Figure 3 Power Dissipation

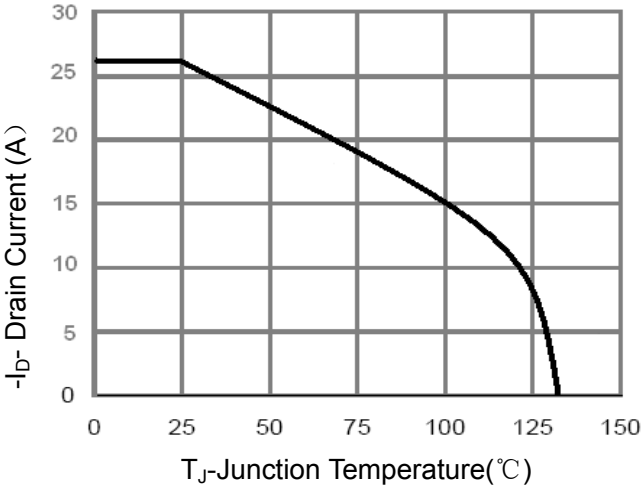


Figure 4 Drain Current

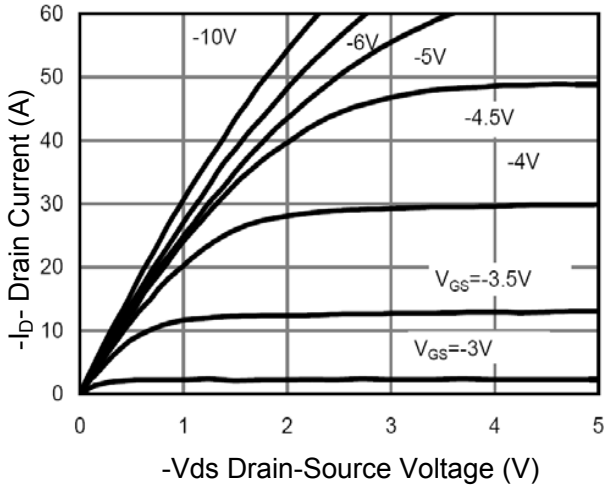


Figure 5 Output CHARACTERISTICS

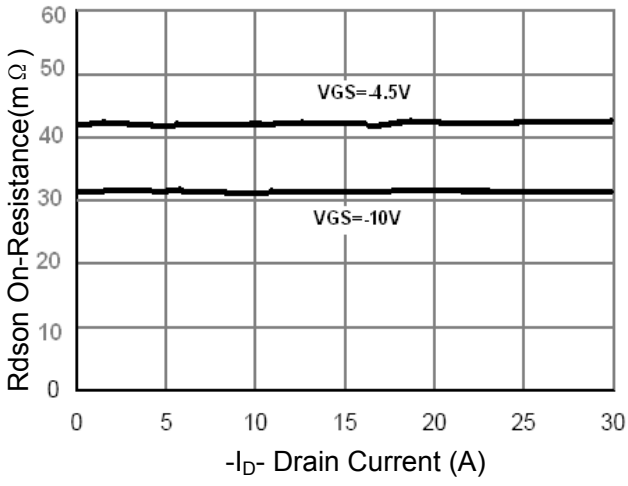


Figure 6 Drain-Source On-Resistance

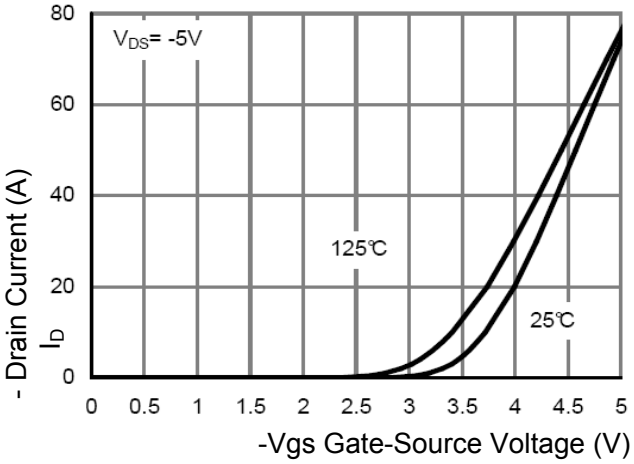


Figure 7 Transfer Characteristics

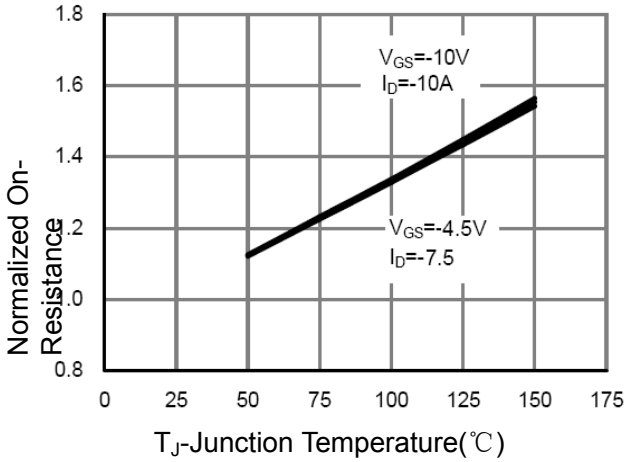


Figure 8 Drain-Source On-Resistance

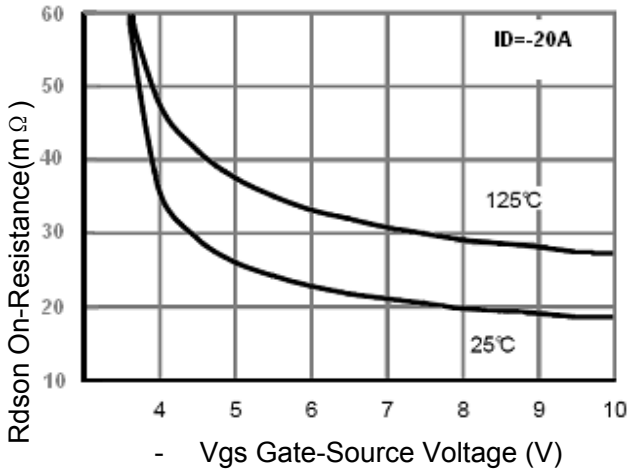


Figure 9 Rdson vs Vgs

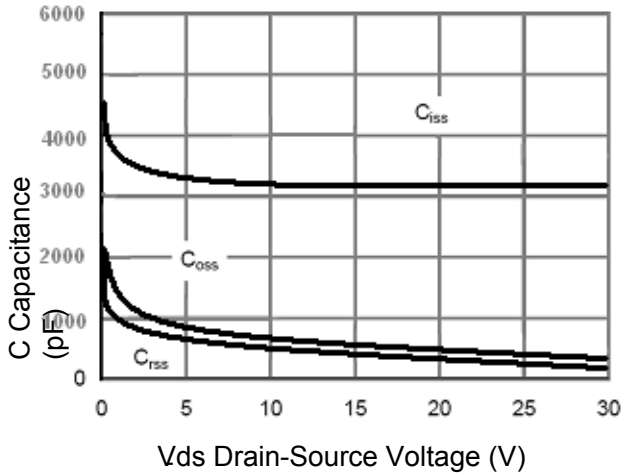


Figure 10 Capacitance vs Vds

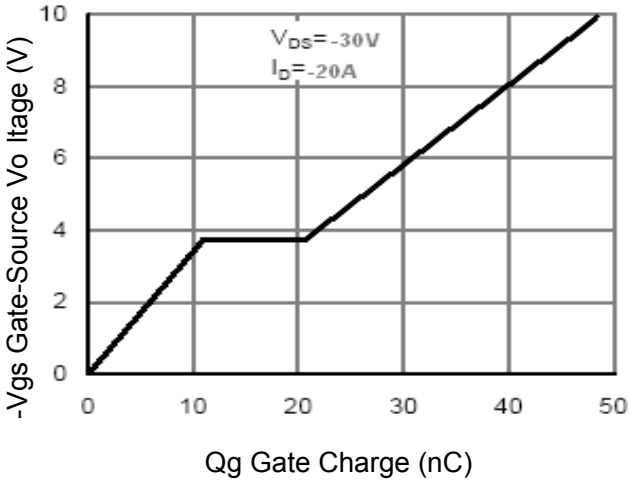


Figure 11 Gate Charge

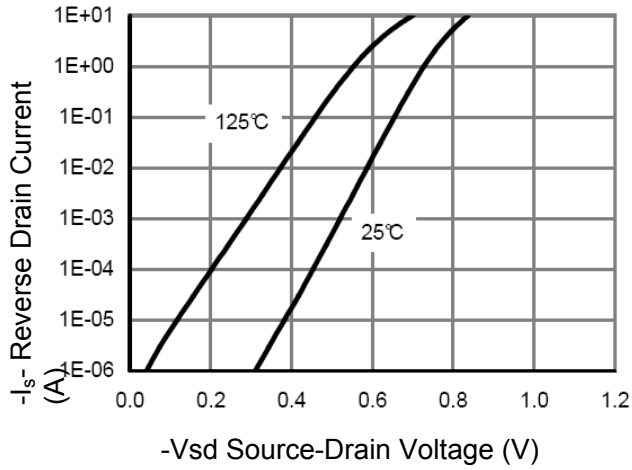


Figure 12 Source- Drain Diode Forward

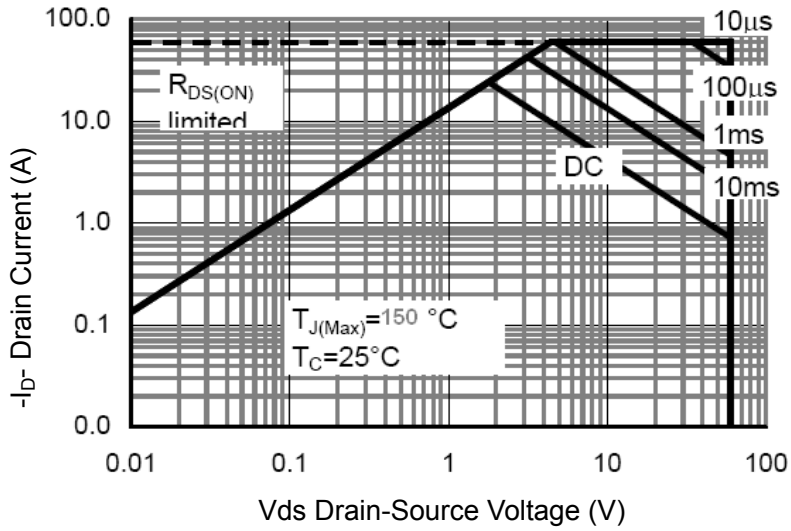


Figure 13 Safe Operation Area

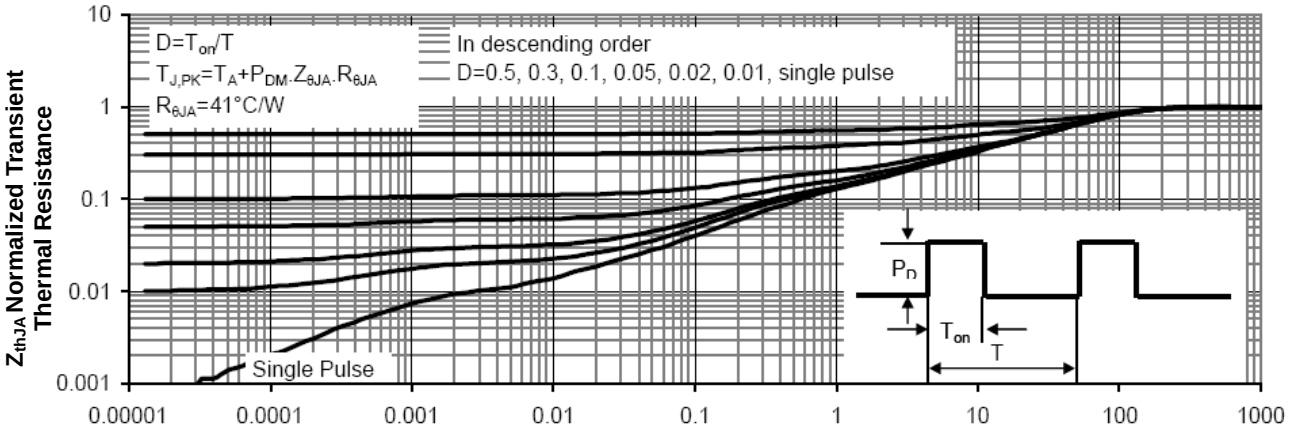
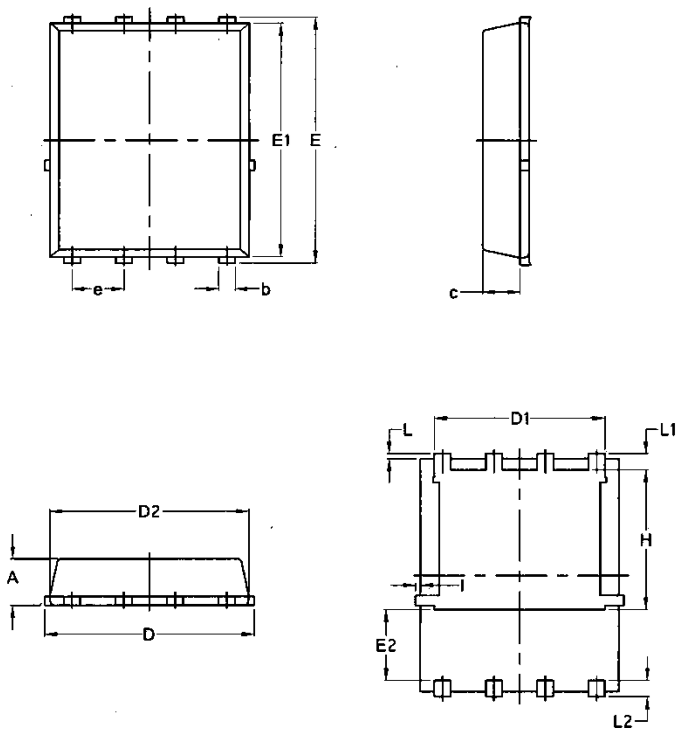


Figure 14 Normalized Maximum Transient Thermal Impedance

Package Mechanical Data-DFN5*6-8L-JQ Single



Symbol	Common			
	mm		Inch	
	Mim	Max	Min	Max
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.824	0.0970	0.0324	0.082
D	4.80	5.40	0.1890	0.2126
D1	4.11	4.31	0.1618	0.1697
D2	4.80	5.00	0.1890	0.1969
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	1.60	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0020	0.0098
L1	0.38	0.50	0.0150	0.0197
L2	0.38	0.50	0.0150	0.0197
H	3.30	3.50	0.1299	0.1378
I	/	0.18	/	0.0070